An Evaluation Tool for Standard Cell Libraries under PVT Variation: Application to Sub-threshold Design

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A tool has been developed to compare standard cell libraries in different operating conditions, i.e. different sets of supply voltage, temperature, process corner, and bias voltages. The approach has then been applied to a 0.5 V sub-threshold cell library developed by CSEM to evaluate the effectiveness of adaptive body bias compensation in the Mie Fujitsu 55 nm DDC process [1].

For a digital designer, the relative speed difference between different processes is a useful figure to solve commonly asked questions: First, it allows the designer to estimate the achievable performance of the circuit for a given yield target. Second, knowing the range of variation across anticipated operating conditions is important to decide for a realistic set of constraints for the CAD tools during implementation which has a large influence on the tool runtimes as well as on the achievable performance of the design. Finally when using methods like adaptive voltage scaling or adaptive body biasing there is a need for the designer to evaluate the effectiveness of the chosen compensation approach.

The evaluation is done in three steps: First, the library files are parsed. Second the delay tables are resampled using bivariate spline interpolation across corners to a common load index and a corner specific transition index. The latter one is derived by exploiting the high gain of CMOS circuits: As shown in Figure 1 a buffer chain is constructed, with the same load on each node. An input transition is applied and throughout the chain quickly converges to a characteristic transition which only depends on the operating corner and the chosen load. The implementation is a simple iterative table lookup in the transition tables of the library files which is repeated once for each value from the load index to construct the transition index.

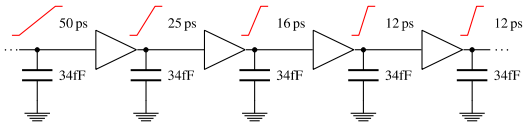

Figure 1: Buffer chain illustrating the converging transition time for a given load.

Finally, after these normalization steps, each delay table entry—in the following called realization *r = {cell, input transition, output load, logic inputs, …}*—of the operating corner OC_l is normalized with the entry of the corresponding realization in a reference corner OC_{ref}, resulting in a relative delay factor α_r:

$$\alpha_r = t_{pd}(r, OC_l) / t_{pd}(r, OC_{ref})$$

In this work a sub-threshold cell library developed by CSEM for the Mie Fujitsu 55 nm DDC process was targeted for analysis, with the goal to evaluate the effectiveness of adaptive body biasing for process, voltage and temperature (PVT) compensation. The body bias voltages have been set based on the result of spice simulations with the goal to achieve an identical drive current across the corners. A commercial library characterization tool was used to derive non-linear delay model (NLDM) representations utilizing the Liberty format across the PVT range with and without compensation.

When analyzing the resulting normalized relative delays α for all realizations without compensation, we observe a wide distribution of the median delay (blue line in the boxes of Figure 2, top). The worst case median exceeds a delay factor of 20 in regard to the reference corner with outliers (black crosses) nearly reaching to a factor of 80. After compensation (Figure 2, bottom) the median delay is pushed back, achieving values close to one. Still, even after compensation, some outliers remain with up to the extreme of 4.3 times the reference delay. These outliers however are rare and for a typical critical path we may only expect a few of them, if at all, which limits their potential effect on the overall timing.

In conclusion, the analysis tool was able to demonstrate the effectiveness of the adaptive body bias compensation approach, illustrating the capability of pushing the corners close together.

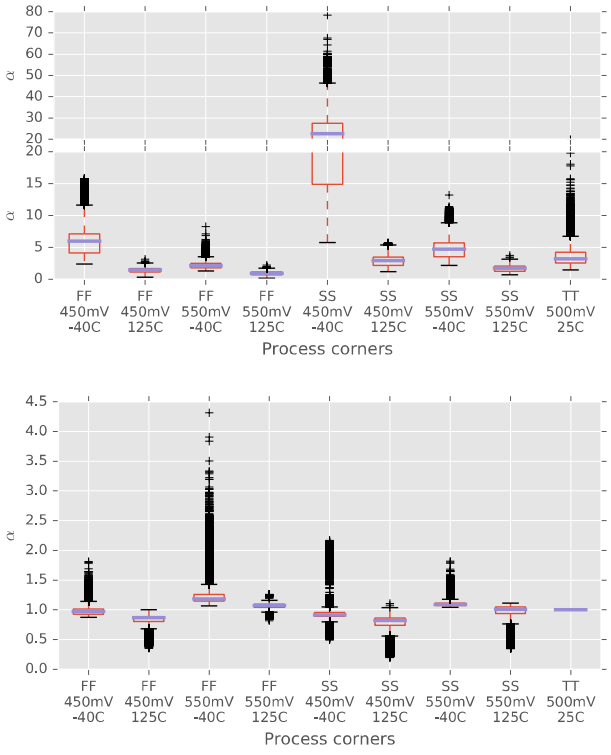

Figure 2: Tukey boxplots of the normalized relative delay α before (top) and after (bottom) compensation. The compensated TT corner has been chosen as OC_{ref} to allow for direct comparability between both plots.

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[1] T. C. Müller, *et al.*, "PVT compensation in Mie Fujitsu 55nm DDC: a standard-cell library based compensation", IEEES3S The IEEE SOI 3D Subthreshold Microelectr. Techn. Unified Conf. (2017).