Sub-threshold Latch-based icyflex2 32-bit Processor with Wide Supply Range Operation

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A 32-bit latch-based icyflex2 processor was integrated in EM Microelectronic Marin ALP CMOS 180 nm technology showing full functionality for supply voltage ranging from 0.37 V (i.e. subthreshold operation) to 1.8 V (i.e. super-threshold operation), over 5 process corners and for temperatures between -25 and 75°C. This possibility to maintain continuous full functionality by adapting the operation frequency and varying the supply voltage makes that design a perfect candidate for adaptive dynamic voltage frequency scaling (ADVFS).

The system micrograph is shown in Figure 1. It includes a latch-based 32-bit icyflex2 controller core [1], 2 kB of RAM, 8 kB of ROM, GPIO, JTAG, SPI and timer peripherals. It can either execute stand-alone functions from the ROM, or boot on an external non-volatile memory via SPI. On-chip debug is possible via JTAG interface.

A tailored standard cell library, as well as RAM and ROM memories were designed and optimized for subthreshold operation. The objective is to ensure a wide supply range operation (WSR), stretching from sub-threshold to super-threshold operation. High-threshold voltage (HVT) transistors were used to reduce leakage. The design was constrained for setup time at the minimum VDD of 0.54 V (corresponding to sub-threshold operation for the HVT transistors) in slow process and low temperature. The maximum VDD considered is 1.8 V. RAM and ROM memories were optimized to reach the same minimum VDD as standard cells to be able to use a single power domain. Optimized high-range level-shifters, allowing the up-conversion from sub-threshold to up to 3.3 V, were inserted in front of output pads of the JTAG and SPI peripherals.

The system performance was measured by running a software self-test (MBIST) of the RAM on the icyflex2 core, the code being stored in ROM. The March C algorithm was executed in around 37'000 cycles for the 2 kB of SRAM. The power consumption of this algorithm is relatively high, considering that the inner loop of the algorithm performs one ROM access, one RAM access and one arithmetic operation (add, sub, or) almost every cycle. The MBIST is also a comprehensive test for all system components as it tests the core as well as the RAM and ROM memories. The MBIST test was run for various temperatures, process corners and frequencies. The result of the MBIST (passed or failed test) is output on the GPIOs and was used to derive the maximum operating frequency.

Reducing the supply voltage logically leads to a reduction of the maximum operating frequency (see Figure 2). We computed the energy (per cycle) by normalizing the power by this maximum frequency. The Minimum Energy Point (MEP) corresponds to where the circuit operates at the highest energy efficiency (usually at a rather low operating frequency). For this circuit, MEP occurs below the threshold voltage, with energy per operation as low as 17.1 pJ/cycle at 19 kHz and 0.37 V. The energy per operation rises to 119.3 pJ/cycle at 1.1 V and 10 MHz, almost 7 times higher than at the MEP, demonstrating the clear advantage of sub-threshold operation in terms of energy as long as the system can cope with the reduced operating frequency.

The proposed icyflex2 processor's MEP was compared very favorably to other state-of art systems (see [2] detailed results).

We have demonstrated that combining latch-based design and sub-threshold allows a very wide supply range of operation. The next step will be to take advantage of these techniques in a fully adaptive system in order to automatically reach an optimal energy efficiency.

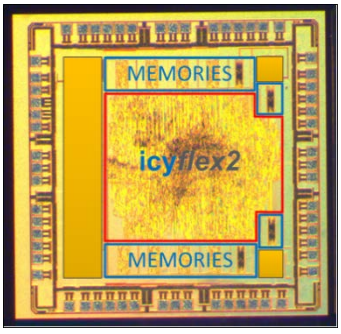

Figure 1: Die microphotograph of the subthreshold system.

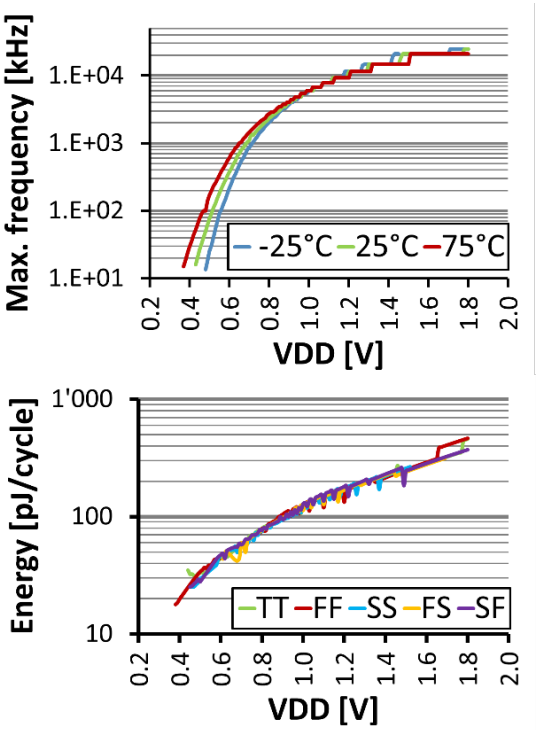

Figure 2: (top) Maximum operating frequency vs. supply voltage for a typical corner chip; (bottom) Energy per cycle measured at maximum operating frequency vs. supply voltage at 25ºC for 5 process corners.

[1] J.-L. Nagel, *et al.*, "The icyflex2 processor architecture", CSEM Scientific and Technical Report (2009).

[2] M. Pons Solé, *et al.*, "Sub-threshold latch-based icyflex2 32-bit processor with wide supply range operation", ESSCIRC (2016).