MiniNOB–Cooperative Sensor SoC for ECG and EIT

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A system-on-chip (SoC) has been developed in a 0.18 µm CMOS process. This SoC is at the heart of a miniaturized wearable system for the continuous measurement of several multi-dimensional physiological signals such as multi-lead ECG (electrocardiogram) and EIT (electrical-impedance tomography). The integrated functions are: communication and synchronization of cooperative sensors, voltage measurement and current injection for EIT, as well as multi-lead ECG measurement.

Cooperative sensing is a patented CSEM's approach for wearables measuring physiological signals, such as bio-potential or bio-impedance. The advantage to the state-of-the-art technology (where a set of passive electrodes is connected to a single measurement unit) is that a high quality signal can be measured with dry electrodes by using only one non-shielded (and possibly even non-insulated) conductive electrical connection. In addition, each sensor is running autonomously and on its own battery, which makes easy the sensing of additional signals, such as optical or acoustic signals. Moreover, adding more cooperative sensors to the system is easy and makes therefore the approach scalable and configurable.

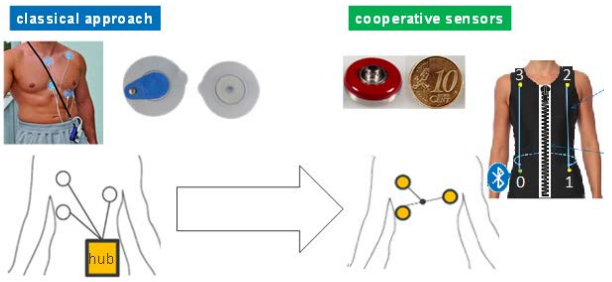

Figure 1: Classical approach and cooperative sensors (MiniNOB).

In the MiniNOB system, which is designed to measure ECG and NOBP (non-occlusive blood pressure), four cooperative sensors are used (see Figure 1, far right). Sensor 0 acts as master and collects the data from all other sensors prior to transmission through BTLE (Bluetooth low energy). Furthermore a current is injected in order to control the reference node (sensor 1) to ground potential. Sensors 1 and 2 measure the body surface potential (BSP) and impedance (IMP) signal, and send the data to the master through the communication channel. Sensor 3 injects a current and also sends digitized BSP measurement data to the master. The entire system is running on a single wire. The body is used as the return path. This is possible as the BSP, IMP and communication signals are located in different frequency bands (see Figure 2).

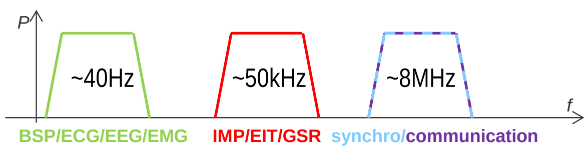

Figure 2: Frequency band for BSP, IMP and communication.

A system-on-chip (SoC) was integrated such that it can be configured as any of the four sensors. It contains two main blocks: communication and sensing. The communication block (see Figure 3) can be configured as either master or slave. In the latter case, a dual-loop clock and data recovery (CDR) block extracts the sampling clock from the incoming data pulses. Otherwise an internal reference clock is used. Note that since the communication pulses share the channel with the 50 kHz signal used for impedance measurement, a 3rd order high-pass filter was needed before any communication pulses can be detected. In the digital TX part, data whitening is applied prior to Manchester encoding. For every 1000th bit, the start of a new frame is indicated by a violation in the Manchester code ("code break"). Finally the data is pulse-modulated, i.e. data '1' is transformed into a positive pulse followed by a negative pulse. Data '0' is transformed into a negative pulse followed by a positive pulse.

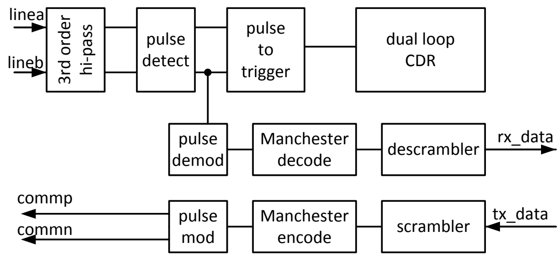

Figure 3: Block diagram communication part.

In the digital RX part, the detected pulses are demodulated, Manchester-decoded and finally descrambled. Code breaks are used to synchronize to the data frame.

The sensing part of the SoC is shown in Figure 4. The BSP measurement chain consists of a pre-amplifier, a passive low-pass filter, an instrumentation amplifier, and an ADC. The closed-loop gain (26 dB to 40 dB) and hi/low pass cutoff frequency (0.67 Hz resp. 40 Hz) of the pre-amplifier are set by external components.

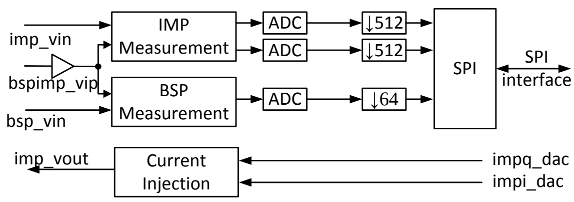

Figure 4: Block diagram sensing part.

The IMP measurement chain consists of a pre-amplifier with filter, a de-modulator, a passive filter, and an ADC. First the in-band signal (49 kHz to 51 kHz) is amplified and out-of-band signals are suppressed. The purpose of the current injection block is to deliver a modulated current in the 50 kHz band. It consists of a modulator, a filter and a voltage-to-current converter by means of an external resistor.

The SoC has been implemented in a 0.18 µm CMOS technology. Samples are expected to be evaluated in the fall of 2016.