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# Sub- and near-threshold design for ultra low-power applications

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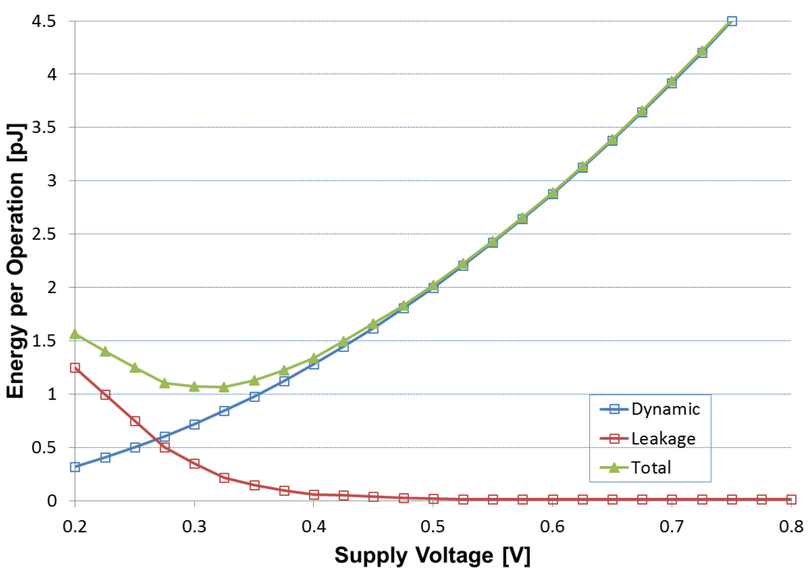
**The main goal of sub- or near-threshold design (i.e. integrated circuits with a supply voltage lower or just above MOS transistor threshold voltage, or $V_T$) is to reduce the power consumption by decreasing the supply voltage. Working at lower voltages than regular circuits opens the door to better power efficiency. However, at these low voltages, IP libraries need to be revisited to ensure correct operation and be optimized for a specific process, supply voltage, operating frequency or static power consumption. CSEM has carried out several designs for several CMOS processes and foundries, resulting in multiple new libraries and specific design techniques.**

## Sub- and near-threshold operation




$$P_{dyn} = \alpha \cdot f \cdot C \cdot V_{dd}^2$$

$$P_{stat} = I_{off} \cdot V_{dd}$$

Energy per operation:

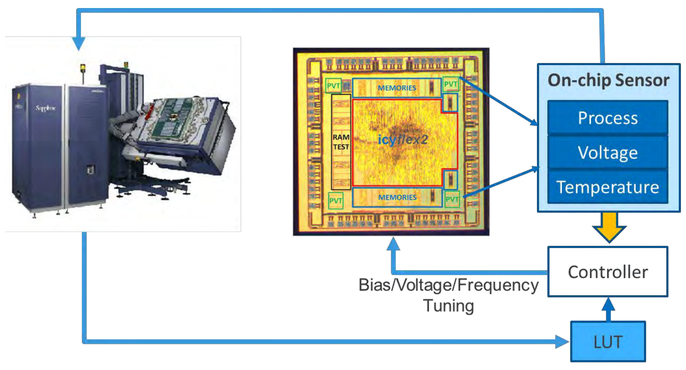
$$E = \frac{P_{tot}}{f} \text{ [J]}$$

Combining optimized libraries and proper design techniques a factor of 3-5x in energy can be gained compared to a nominal supply implementation.

## Adaptive Voltage-Frequency-Bias

Several chips have been integrated by CSEM to validate sub-$V_T$ libraries.

Due to the higher variability in sub-threshold (local mismatch) an adaptive approach is recommended (ADVBFS) to optimally use the technology resources:




## Examples of applications

Sub-$V_T$ design is specifically well suited for the following applications:

- Always-on applications, possibly with short bursts when $V_{DD}$ is raised for greater processing throughput (duty cycling)
- Chips running with energy harvesting (e.g. photovoltaic) to avoid lossy step up/down voltage regulation

**Example applications**

1) Solar-powered wristwatch

with BlueTooth LE transmission

2) Solar-powered IoT intelligent tags

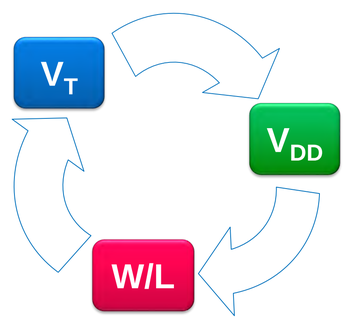

## Building blocks for sub-$V_T$ design

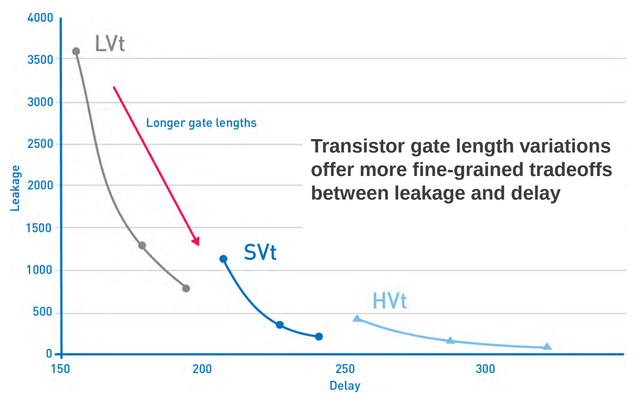
Several building blocks need to be available to support sub- or near-$V_T$ design. These basic blocks have been designed at CSEM:

- ✓ Standard cell library
- ✓ RAM
- ✓ ROM
- ✓ Level shifters
- ✓ Pads
- ✓ Power Management

Libraries can be optimized for several criteria. CSEM has solutions for the following:

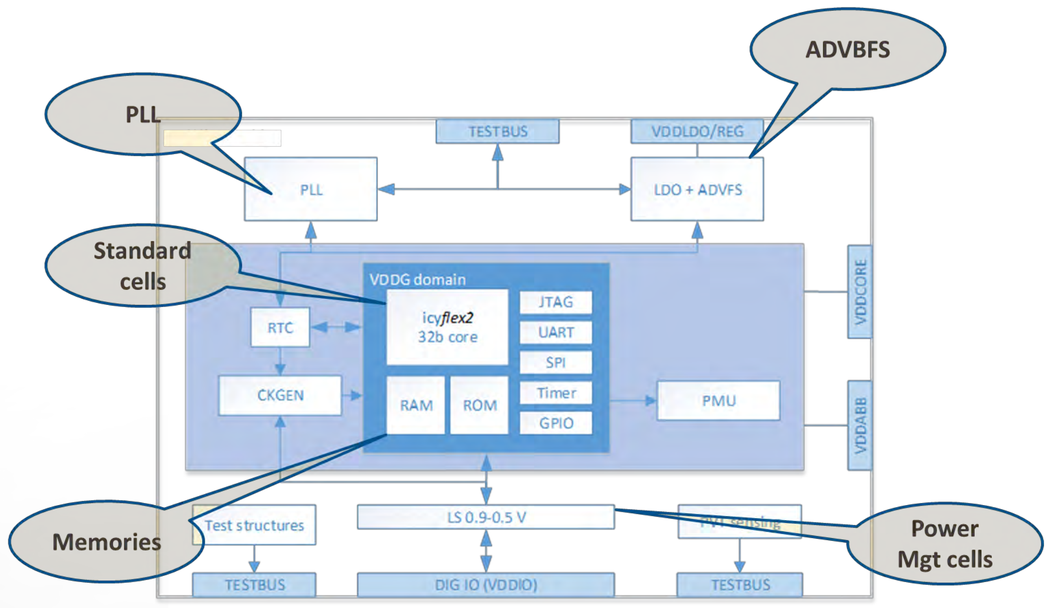
- The lowest possible supply voltage
- The lowest possible leakage while supporting a target frequency




## Industrial collaborations on sub-$V_T$

Among several industrial collaborations, CSEM does collaborate with Fujitsu on the development of libraries and solutions for their DDC 55nm technology.




Thanks to advanced adaptive compensation techniques complete System-on-Chips (SoC) including processors can be operated up to several tens of MHz at a supply as low as 0.5V.