Design and on-Silicon Characterization of a 6T SRAM Memory Operating at Subthreshold Voltage

M. Pons Solé, T.-C. Le, C. Arm, D. Séverac, S. Emery, C. Piguet

Subthreshold designs reduce power consumption by working down to lower voltage levels than classical design (i.e. 0.4 V). This allows for instance a longer battery life, or even better, replacing the battery by energy harvesting (e.g. photovoltaic cells can generate 0.4 V directly). However SRAM blocks limit the minimum voltage at which the whole design can be supplied. SRAM bit-cell noise margins are highly degraded in subthreshold operation due to the increased sensitivity to process, voltage and temperature variations. This motivated the optimization of an SRAM memory for subthreshold operation with special attention to manufacturability. The SRAM on-silicon measurements for a 180 nm technology are presented here.

Subthreshold 6T bit-cell design

The trend for subthreshold SRAM design is to add some or several transistors to the classical 6T bit-cell to overcome low-voltage limitations. In the literature, solutions can be found spanning from 7T to 14T bit-cells. However, adding transistors leads to more variability, noise and power consumption. Our proposal is to change the read protocol at an architectural level based on the "Random Access Memory" CSEM patent [1] where the read access is performed from a single side (Figure 1). Both bit-lines (*bl1* and *bl2*) are used for a write operation, however only *bl1* is used for reading. Doing so, the reading static noise margin is improved as only one side of the internal loop is aggressed. Moreover no sense amplifiers are required as full voltage swing is applied to the bit-line and only simple tri-state gates are used. This also simplifies and increases the robustness and manufacturability at subthreshold voltage. Bit-cell transistors are also upsized to optimize them for subthreshold effects. This optimization is based on our previous works for subthreshold standard cell design [2]. For this work in 180 nm, the minimum channel length has been determined to be 420 nm. To refine transistor sizing, Spice simulations have been performed taking into account process variations, voltage from 0.4 V to 0.9 V and temperature from -40°C to 125°C. The worst read static noise margin is 40 mV for 0.4 V operation and over 130 mV for 0.9 V (for 0.4 V and a minimum channel length sizing of 180 nm, it is 20 µV and the bit-cell is not operating anymore).

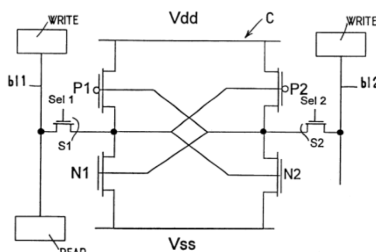

Figure 1: 6T bit-cell. WRITE and READ circuits indicated as boxes.

Subthreshold 1 kib SRAM memory design

The 1 kib SRAM block (total area of 22'350 µm^2) includes:

- A full custom decoder implemented using standard cells able to sustain the bit-cell subthreshold voltage operations
- Pre-charge switches and tri-state gates for reading controlled by an "output enable" signal to decrease read power consumption
- Write-mode tri-state gates to drive the *bl1* and *bl2* signals controlled by "byte enable" signals to decrease write power consumption
- A bit-cell array composed of 16 rows of 8 bytes that can be individually addressed for a total of 1 kib memory size

On-silicon characterization of the SRAM

The SRAM was tested using a March algorithm that activates all the addresses and forces worst-case paths. Measurements at room temperature for supplies up to 0.6 V are shown in Figure 2. The SRAM is 100% functional (i.e. all the output bits tested in the March test are correct) at a minimum voltage of 0.27 V, with a maximum frequency of 530 Hz, with only 3.1 nA of total current and 2.4 nA of leakage. It can be observed how the ratio of total and leakage current is small for sub-threshold operation (that is why bit-cell robustness is critical). This ratio increases with supply voltage. For lower voltages and higher frequencies, correct read and write operations were observed, however the March test did not complete satisfactorily. As expected, the bit error degradation occurs when reaching deep sub-threshold supply voltage levels (see Figure 3).

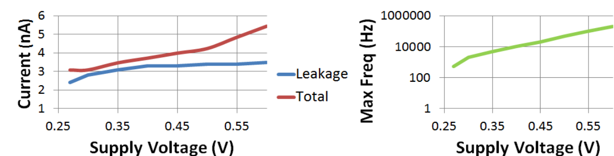

Figure 2: SRAM leakage, total current and maximum frequency.

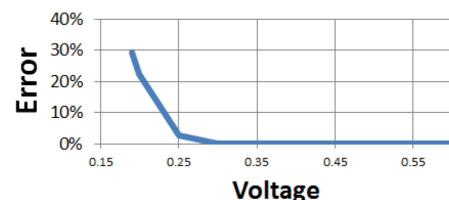

Figure 3: SRAM measurements for bit errors degradation.

Conclusion

A 1 kib 180 nm 6T subthreshold SRAM has been designed with a focus on manufacturability, then integrated and measured satisfactorily. The design operates without errors down to 0.27 V which allows a seamless use of this SRAM block in combination with energy harvesting techniques.

[1] J.-M. Masgonty, *et. al.* , "Random access memory," US 6366504 B1 patent, (2002)

[2] M. Pons, *et. al.* , "Ultra low power standard cell design using planar bulk CMOS in subthreshold operation," in the International Workshop on Power And Timing Modeling Optimization and Simulation (PATMOS), (2013) 9