A Versatile Sensor Interface for IO-Link Applications

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The actual IO-Link Standard version 1.1 was launched at the end of 2010. In the meantime, IO-Link has applied for acceptance as an IEC-norm, and became a world-wide accepted norm in automation. CSEM designed a sensor interface composed of a novel versatile capacitance to voltage converter (C2V), two programmable gain amplifiers (PGA) with sample and hold (SH) and a low-pass filter (LP) incorporated in HMT Microelectronics' HMT872 ASIC. This ASIC also encompass an 18-bit ADC, a 14-bit DAC, a temperature sensor, a serial-parallel interface (SPI) and an IO-Link interface.

IO-Link is the first standard IO technology worldwide (IEC 61131-9) for the communication with sensors and actuators [1]. It is based on the long established 3-wire sensor and actuator connection without additional requirements.

The sensor interface is illustrated on the following block-schematic together with the whole IO-Link ASIC.

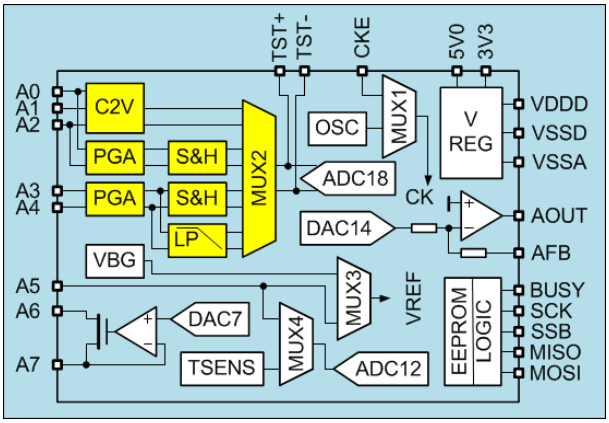

Figure 1: Block-schematic of the HMT872 IO-Link compatible ASIC with the sensor interface part highlighted.

The ASIC includes the following characteristics:

- Wide temperature range from – 40 to + 125°C
- Versatile Programmable Gain Amplifier (PGA) stage with 14 µV input referred noise and programmable gain from -6 dB to 48 dB
- Capacitance to voltage converter with high input capacitance range from 1 pF to 100 pF and tuneable bandwidth up to 10 kHz
- High precision DAC for actuators yielding 14-bit resolution with 20 kHz sampling rate
- High resolution ADC: From 12 effective bits and 10 kHz bandwidth to 18 effective bits and 1.2 kHz bandwidth

The most unusual circuit of the ASIC is the C2V converter. The challenge of this block is to handle a wide range of capacitive sensors. Differential capacitive sensors have a mid-point electrode that is not trivial to handle with a differential circuit. It has been made possible only with a dedicated multi-phase structure comprising a difference differential amplifier (DDA) that is used alternately on either input pairs. The result is a truly differential circuit with inherent correlated double sampling operation that suppresses the 1/f noise.

The C2V block can handle various differential or single-ended capacitive sensors, with a total capacitance of up to 100 pF.

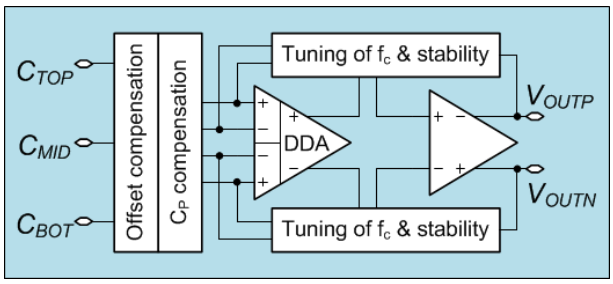

Figure 2: Simplified block-schematic of the fully differential C2V.

All capacitive sensors possess both sensitive and parasitic capacitances (C_S and C_P). In order to ensure linearity, the C2V interface can compensate C_P up to 40 pF with a resolution of 10 bits. There is also an offset cancellation of 16 pF with 10 bits resolution. Finally, a tuning that acts on the cut-off frequency f_c is used to ensure the stability of the circuit for large capacitance sensors. The tuning strategy dispatches a total capacitance amongst the various pairs of the differential circuit's capacitors such that none of it is wasted. This results in a wide sensor capacitance range and optimal noise performances.

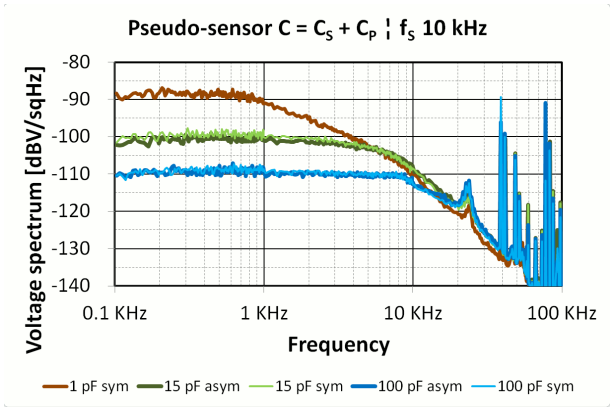

Figure 3: Noise measurement of the C2V with pseudo-sensors.

The noise measurements above are made with pseudo-sensors made of fixed capacitors. After compensation (i.e cancellation) of C_P, this is the active sensor capacitance C_S which is relevant for the noise estimation.

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• HMT Microelectronic AG, Switzerland
•• EPFL, ESPLAB, Switzerland

[1] IO-Link System Description – Technology and Application, www.io-link.com