A Miniature Timing Module Embedding its XTAL within the CMOS Substrate

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MEMS oscillators have recently successfully entered the timing market owing to the packaging revolution enabled by wafer scale technologies. This paper explores how XTAL resonators could similarly benefit from such technologies with the demonstration of a miniature timing module.

One of the main goals of the Go4Time EC-funded FP7 project was to demonstrate how post-CMOS wafer scale technology could be applied to the packaging of miniature tuning fork XTALs. Embedding the later directly within the CMOS substrate leads to the ultimate miniaturization of timing modules which are at the heart of almost any electronic system. In order to develop a versatile module, 131 kHz XTALs were combined with 2 GHz BAW resonators to enable the generation of both a low power sub-μW real time clock (RTC) and of an on-demand low jitter clock of high spectral purity that could support the requirements of radio applications such as for Bluetooth Low Energy (BLE). Furthermore, the hybrid packaging approach which was developed is applicable to any sensor that should be put in intimate contact with its CMOS read-out circuit in an air tight or vacuum-sealed cavity.

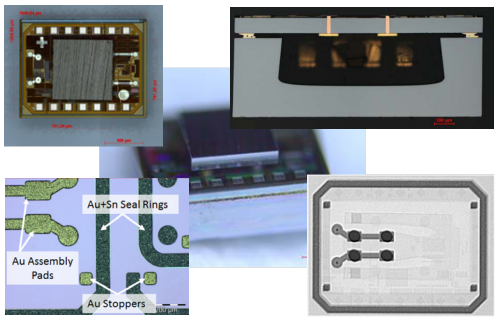

Figure 1: Timing module photographs: center, side view showing wafer stack and BAW die on top of CMOS; top-left, top view showing IC IOs, RDL and TSVs; top right, cross section revealing TSV, XTAL, and cap; bottom-left, CMOS backside, bottom right, X-ray picture.

Pictures of the fabricated modules, which were produced on 8" wafers following a standard 180 nm CMOS process flow, are shown in Figure 1. In order to generate through silicon vias (TSV), holes are first etched from the CMOS side of the wafers to a depth of 100 μm through the BEOL metallization and silicon before being filled with copper. A redistribution layer (RDL) is then deposited and patterned to redirect the original frontside circuit IOs to the wafer backside with the help of the newly formed vias. The later are revealed after grinding the CMOS substrate, which has been previously glued to a temporary holding glass wafer, down to a residual thickness of 100 μm. A backside Au-RDL is then electro-plated to connect the TSVs, define the XTAL landing patterns and form mechanical stoppers. Gold-tin seal rings are subsequently plated and Au-studs are bumped on top of the landing patterns completing the post-CMOS processing. The XTALs are then individually attached using a die bonder. In parallel, cap wafers plated with Au seal rings of matched geometries are formed by etching cavities to accommodate the protruding XTALs after the wafers are bonded together at 280°C [1]. Eventually miniature BAW resonators are reflow-soldered on pads lying on the front CMOS side after removal of the temporary bonded glass wafer. The resulting complete timing modules measure only 1.6x1.2x0.6 mm^3, hence about the dimensions of a single miniature radio XTAL.

Wafer level measurements of the timing modules prior to BAW assembly were performed at room temperature in order to assess the packaging manufacturing yield. Figure 2 provides two wafer maps depicting the yield. The multi-layer mask CMOS design was shared equally between the XTAL/BAW and a Silicon Resonator-based version arranged in a chessboard configuration (related black sites not populated). Dummy sites containing foundry test structures are colored in yellow. Only the central wafer area was populated with XTALs forming 2600 XOs. White cells denote know-good dies (KGD) with fully functional, hence properly sealed and interconnected XOs. Red cells represent non-functional DUT while blue cells are those having suffered from probe-card contacting/alignment issues. Overall, the yield reaches ~70%, while large areas are found mostly defect free. The mean core current consumption of the 131 kHz XO from the best wafer reached ~60 nA with a deviation of 12%. This is 2.5 times higher than what was obtained with XTALs packaged in standard ceramic packages, glued on a standard CMOS wafer and wire-bonded to the ICs. The difference is due to a larger package parasitic capacitance from the TSV and RDL and a higher residual cavity pressure lowering the Q-factors.

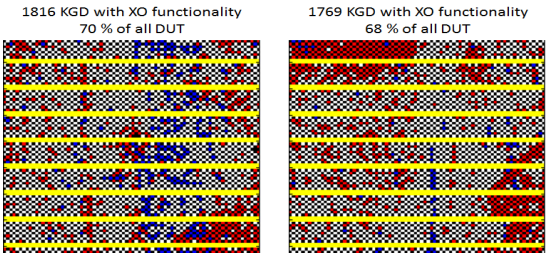

Figure 2: Wafer map showing timing module manufacturing yield.

This work demonstrated the potential manufacturability of a leading edge European timing solution. It was performed within the project Go4Time that was funded by the EC FP7 research program. The consortium led by CSEM was formed of Micro Crystal, ST, Fraunhofer IZM, VTT, Polimi and TuD.

• Micro Crystal AG, Switzerland
•• Fraunhofer IZM, Germany
••• VTT Technical Research Centre of Finland LTD, Finland
* STMicroelectronics, Italy

[1] K. Zoschke, *et al.*, "Application of TSV integration and wafer bonding technologies for hermetic wafer level packaging of MEMS components for miniaturized timing devices," in Proc. IEEE Electronic Components and Technology Conference, (2015) 1343