A 1 M-Pixel 2000 Frames/s Image Sensor

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A high-speed image sensor implementing 11 bit ADCs and pixels with a high Full-Well-Capacity of 150 ke- has been developed. It is capable of outputting up to 2000 frames/s at a 1 us row-time in global shutter mode. This sensor fits the needs of many industrial, medical and automotive applications requiring fast, high Dynamic-Range and high-SNR cameras. The building blocks have been developed in a tower 0.18-µm CMOS process and serve as a basis for further high-speed camera projects as required for industrial automation, optical coherence tomography or process analysis.

High-speed image sensors are widely used for industrial, medical and automotive vision applications where fast moving objects have to be captured and analyzed. Most high-speed sensors on today's market implement a global shutter exposure to capture smear free images, 10 or 11 bit ADC's for reaching ~60 dB Dynamic Range and achieve row-times between 1-2 us. However, due to the reduction of the pixel pitch from 12 µm to about 6 µm, the pixel Fill-Factor and Full-Well-Capacity is lowered. Typical Full-Well-Capacity of these sensors is in the range of 20 ke- resulting in SNR levels of ~40 dB. This low SNR level is not sufficient for many applications because of the resulting low image quality.

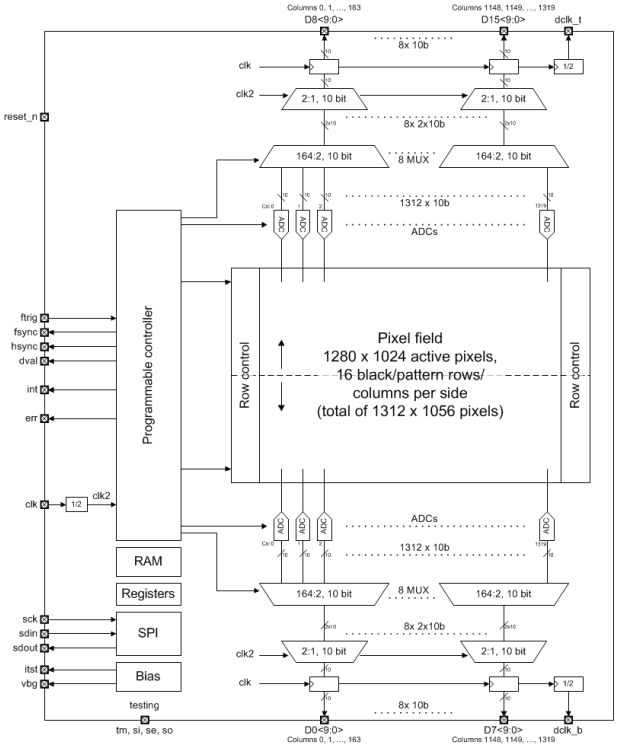

Figure 1: Sensor architecture of the 1.3 Mpixel sensor.

As part of the EU-project "VIAMOS—Vertically Integrated Array-type Mirau-based OCT System" we have developed an image sensor with a 12 µm pixel pitch and a capacity as high as 150 ke-, achieving an SNR of ~51 dB, and including a readout path with a typical row-time of 1 us. This high SNR and short row-time is a strong requirement for our EU partners, whereas the Dynamic Range (>55 dB) is of lesser importance because the illumination level on the sensor pixel field is mainly constant.

The design is based on IP's developed in [1]. To reach the targeted 2000 frames/s a top/down readout architecture with 2 ADCs per column has been implemented. With this method the readout speed can be doubled (see Figure 1).

A major design effort has been spent on the digital backend to reach the 160 MHz clock speed within the big sensor area of 20 mmx20 mm. The sensor is packaged in a custom 356-pin LGA package and evaluated in a custom made test-bed (see Figure 2).

Different types and variations of pixels have been implemented in several test columns of this sensor. This includes pixels with LOG-functionality and pixels targeted for fluorescence lifetime imaging or time-of-flight applications. These pixels together with the blocks developed in this project will serve as a basis for future image sensor developments at CSEM.

The sensor has been evaluated according to the well-known EMVA1288 standard (Standard for image sensor characterization). The measured figures of merit are excellent and exceed the requirements given by the initial specification:

- Full-Well 137 ke-, Dynamic Range: ~60 dB, SNR: 51.5 dB
- Gain 177 e-/DN, Lag: 0%
- PRNU: 0.2%, Non-Linearity: 0.5%
- QexFF@600 nm: 0.5

This results in an excellent video quality which has been demonstrated in a high speed video capturing a rotating fan.

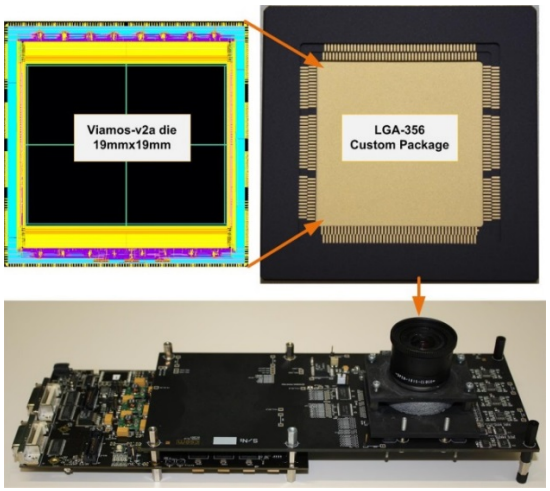

Figure 2: Sensor, test-bed and evaluation environment.

Thanks to the great contribution of all project members and our EU partners, this project can be characterized as a success.

[1] Y. Zha, *et al.*, "A 256 x 256 pixels 4000 frames/s image sensor" CSEM Scientific and Technical Report, (2014) 122