A 60 GHz FMCW RADAR-on-Chip Front-end Integrated in 22 nm CMOS

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CSEM is developing a flexible 57-66 GHz FMCW RADAR IP to be integrated into RADAR-on-Chips for low-power miniature MIMO systems targeting portable and/or long-autonomy short-range applications. We describe here a first integration in 22 nm FDSOI CMOS technology of an LO generation associated with 2x Tx & 2x Rx front-ends.

RADARs take advantage of wideband operation for high resolution and good SNR. In the available worldwide license-free bands, two multi-GHz bands can be considered: the 6-8.5 GHz UWB band and the 57-66 GHz band. The UWB band is of interest for low-power operation and easier integration. However, it is more limited with respect to output power, and range resolution. For miniature systems, it is also limited in angular resolution because of the longer wavelength and relative bandwidth that necessitate much larger antennas.

Compared to FMCW, Pulsed-RADARs, are simpler and less sensitive to Tx-to-Rx isolation. They are however limited in average output power because of the high duty-cycle ratio and limited peak voltage associated with integrated technology. Low-power operation also precludes the use of multi GS/s high-dynamic ADCs in Rx: this lowers efficiency because less constrained ADCs are usually associated with distance or dynamic range sweeping, i.e. multiple pulses per range acquisition are needed. FMCW does not suffer from this approach. Additionally, for reduced constraints in terms of energy per acquisition and/or low required acquisition rate, high duty-cycling ratio remains possible [1].

For these reasons, we are integrating a flexible LO generation for operation over the 57-66 GHz band based on an ADPLL. This provides a tunable sweep duration down to 1 ms and a wide closed-loop bandwidth to cope with frequency pulling while maintaining a good sweeping linearity. The LO generation is based on a quadrature DCO swept at carrier frequency in order to minimize Tx silicon surface. Direct quadrature down-conversion is also implemented to minimize Rx silicon surface. A 1-10 MHz chopper is implemented to modulate the transmitted signal in BPSK, in order to eliminate the DC and the DCO-to-Rx leakage, as well as to reduce flicker noise. Different chopper frequencies are used per Tx to separate them on the Rx side by correlation in digital domain.

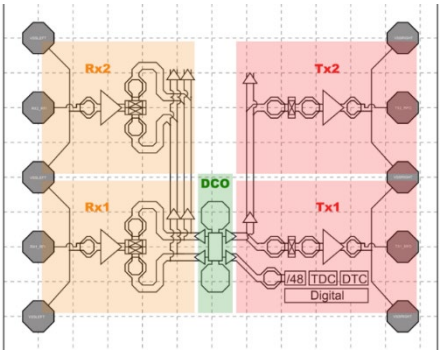

Figure 1: Block diagram of the core.

As illustrated in above Figure 1, 2x Rx & 2x Tx have been integrated to validate a MIMO scheme. The architecture and layout are scalable: more Tx and Rx slices could be added on the LO distribution paths to address different cost/resolution trade-offs.

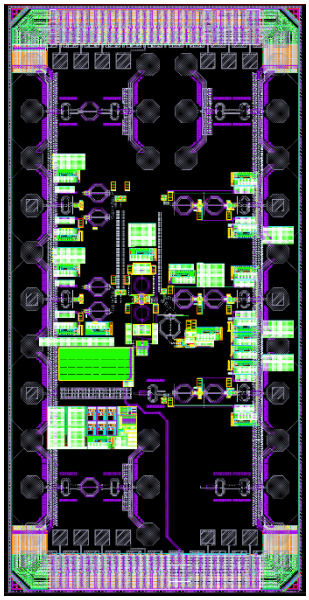

Figure 2: 1.25 x 2.5 mm² test chip in 22FDX.

Figure 2 above depicts the circuit integrated in a 22 nm FDSOI CMOS from Global Foundry, which offers good performance at 60 GHz and the possibility to also co-integrate powerful and efficient digital processing. LDOs and various RF test structures have also been integrated for characterization. However, the Rx low-IF amplification, filtering and the ADCs are off-chip for the moment. The LO generation has a surface of 0.2 mm² and each Rx or Tx has a surface of 0.2 mm² including Ø 90 µm 200 µm-pitch pads that are planned for use in characterization via probing, but will also be used in the future for flip-chip assembly.

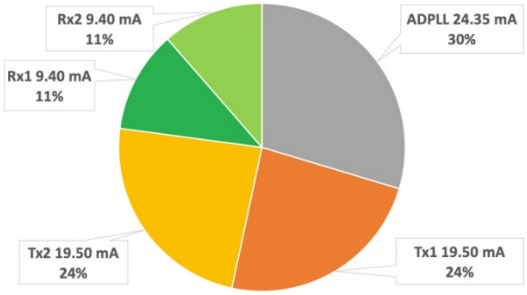

Figure 3: Current consumptions with 0.8 V voltage supply.

For the next integration, we plan to work on reducing the power consumption illustrated in above Figure 3 and completing the system up to ADCs.

[1] Yao-Hong Liu, *et al*., "A 680 µW Burst-Chirp UWB RADAR transceiver for Vital Sign and Occupancy Sensing up to 15 m distance", ISSCC (2019).