An Ultra-low-power System-on-Chip with Adaptive Body Bias

M. Pons Solé, L. Zahnd, Y. Liechti, J.-L. Nagel, V. Moser, E. Azarkhish, R. Cattenoz, T. Mavrogordatos, C. Müller, B. Sporrer, K. Badami, N. Gerber, V. Kopta, E. Pérez Serna, N. Scolari, S. Devise, D. Manic, N. Raemy, S. Emery

The System-on-Chip (SoC) developed is optimized for ultra-low-power applications with increasing battery life constraints. It operates in near-threshold region at 0.6 V and combines user-configurable power management unit (PMU) and bias generator circuits to implement automatic adaptive body bias (ABB) regulation over process, voltage and temperature (PVT) for the icyflex-V core and its memory. It also includes on-chip the icyTRX Bluetooth radio to provide wireless connectivity and ADC/DAC interfaces for sensor applications. Technology used is USJC 55 nm C55DDC which is tailored for low power and body bias control.

ABB mechanism uses transistors body potential as a knob to dynamically control SoC speed and consumption. Reverse bias is used for low-power cases and forward bias is used for high-speed. Figure 1 shows the ultra-low-power SoC implementing ABB. It includes multiple CSEM's designs: 1) icyflex-V [1] (RISC-V based, with 256 kB RAM and 4 kB ROM), 2) icyTRX [2] Bluetooth, 3) low voltage ADC/DAC IPs and 4) PMU and Bias Generator that implement the novel automatic ABB. Thanks to ABB, users can dynamically configure multiple modes of operation of the SoC and control the speed and consumption trade-off. Modes are defined by setting the target clock frequency (e.g. kHz range for Slow mode, MHz range for Fast mode). ABB automatically provides robust operation over PVT for these modes of operation.

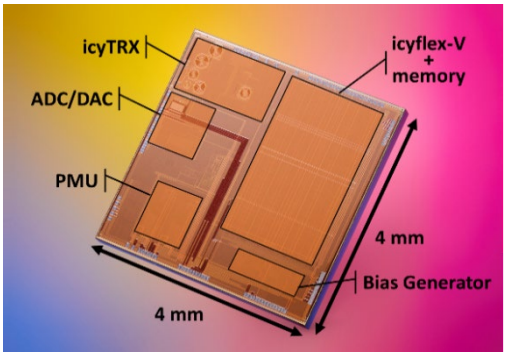

Figure 1: SoC microphotograph.

The different blocks in the SoC can be powered-off using standard power switches and power can also be optimized using ABB. RAM architecture implemented on the SoC is an example of the low-power configurability that can be achieved using ABB. The 256 kB are divided in multiple banks that can be biased independently. When the software requires limited memory, only the minimum size of RAM is active (e.g. configuring Fast or Slow mode) and unused RAM banks are kept in Retention mode. Pushed reverse bias is used for these RAM banks in Retention. These banks cannot be accessed but they hold the data and consume as low as 1 pW/bit. Low-power (for Slow and Retention modes) and high-speed (for Fast mode) versions for both PMU and Bias Generator circuits also coexist on-chip. Users can directly select the versions to use or just select the mode of operation (Fast, Slow or Retention mode) and the suitable versions are automatically activated (the others are powered-off for current consumption reduction). Users can also define a frequency target. The Bias Generator circuit will automatically regulate bias voltages and the clock to ensure functionality over PVT. This Bias Generator circuit is an evolved version from previous works [3] but in this new version a Frequency-Locked Loop circuit (FLL) is used to self-adjust the bias generation and the clock frequency. For that purpose, the FLL includes an oscillator with configurable length that replicates the critical path of the SoC. Mode switching in real-time is supported, allowing the system to adapt to different application phases and obtain optimum consumption results. The SoC can switch for instance from Fast to Slow mode or from Fast to Retention mode and vice versa at any time in the execution of a software. A mode switching specific circuitry takes care of bias voltage continuity over time (avoiding unwanted steps in the bias voltages) and gates the clock while bias voltages are varying (avoiding clock glitches). Figure 2 depicts the SoC's demonstrator. In the application, the SoC is by default in Slow mode (50 kHz setting) and switches to Fast mode (8 MHz setting) using an external trigger (from the Pressure Sensor or the Microphone). Temperature, humidity and current consumption are measured by sensors on-board that are sampled by the on-chip ADC. They are then sent using the icyTRX radio and displayed on a tablet. Power consumption is 10 µA for the Slow mode and 250 µA for the Fast mode. For long periods of inactivity, Retention mode is configured (using pushed reverse bias for the blocks) and consumes 1 µA. In this mode, memories hold the data and SoC clock is gated until the application resumes (for instance, from an external trigger or from an internal timer running on an ultra-low power always-on 32 kHz clock).

Figure 2: Demonstration board (credit card format).

This ultra-low-power SoC with novel automatic ABB provides robust operation for multiple modes of operation over PVT and can be configured by the user depending on the application needs to obtain best current consumption results. The SoC also provides wireless connectivity and sensor interfaces.

[1] J.-L. Nagel, *et al*., "icyflex-V-a New Ultra-low-power Processor based on RISC-V Architecture", CSEM Scientific and Technical Report (2019) 116.

[2] V. Peiris, *et al*., "An Ultra-low-power Bluetooth Smart Integrated Solution", CSEM Scientific and Technical Report (2012) 97.

[3] D. Séverac, *et al*., "A 0.5 V Near-Threshold Microcontroller Robust over PVT Variations", CSEM Scientific and Technical Report (2017) 142.