High Thermal Conductive Die Attach Material for High-power Semiconductor Devices in Space Applications

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High thermal conductivity of materials used for assembly of high-power semiconductors are becoming very important, as the power per unit area of these chips are increasing considerably. High power per unit area results in increase of junction temperatures, resulting in a considerable decrease in lifetime of these devices. To improve the conduction of heat away from the chip, high thermal conductivity silver sinter paste was studied as a replacement for AuSn solder for die-attach of GaN and silicon chips for space applications.

The wide band gap of Gallium Nitride (GaN) devices enables them to handle high breakdown voltages. They also show high charge capacity and high saturation velocity which enables them to handle high current loads. Due to these advantages and high-speed switching capabilities, GaN chips have become a choice for many RF applications like mobile communications infrastructure. On the downside, this causes high-power density which in turn results in high junction temperatures (>175 °C). The lifetime of these devices decreases considerably with increase in junction temperature as shown in Figure 1. So, a reduction in channel temperature is critical for a long-term reliable operation.

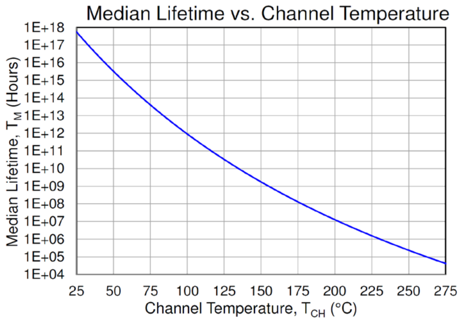

Figure 1: Decrease in lifetime with channel temperature [1].

There has been a lot of research on novel substrates consisting of high thermally conductive materials like different diamond composites and copper alloys. However, only few novel die-attach materials are being investigated. Silver sintering is a promising novel die-attach material for assemblies where high heat transfer is important. Silver sintering was studied as an alternative to Gold-Tin (AuSn) soldering, the main choice for die attach especially in space and photonics applications. This paper compares these two materials and outlines the applicability of silver sinter in space applications.

GaN HEMT transistors and silicon chips with integrated heating and temperature sensing elements were used for the study. Aluminum nitride DBC (direct bonded copper) substrates were used, to provide a good heat transfer away from the chip. 54 silicon chips and 28 GaN chips were fabricated of which half featured silver sinter and the other half AuSn. (Figure 2).

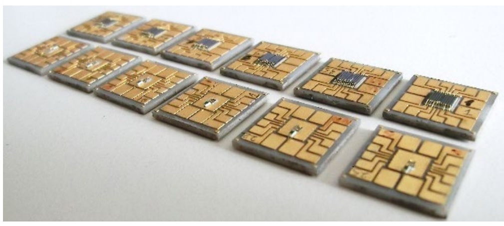

Figure 2: Silicon and GaN Samples after assembly.

Temperature measurements were conducted while powering up the silicon chip to different power levels, to compare the heat transfer in chip assemblies made using AuSn and silver sinter. As shown in Figure 3, silicon chip's surface temperature is ~10% lower for the silver sinter assembled chips compared to chips which were bonded using AuSn solder. This data is based on 27 chips each of solder and silver sinter bonded assemblies.

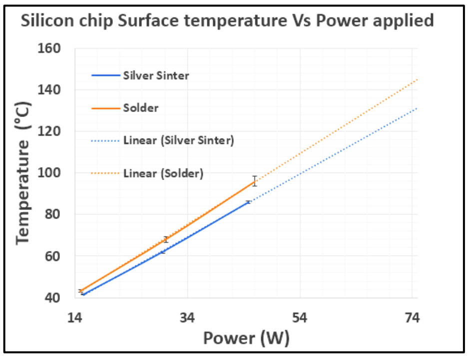

Figure 3: Surface temperature measured on the silicon chip.

It is thought that the lower temperature seen on the silver sintered samples can be attributed to 2 factors:

- Higher thermal conductivity of the silver sinter (>150 W/mK) compared to AuSn solder (57 W/mK)
- The high amount of voiding in AuSn solder joints compared to the porosity in silver sinter which still needs to be accessed.

Silver sinter showed also other clear advantages compared to AuSn. The temperature required for silver sintering is much lower compared to AuSn soldering. The silicon chips assembled using AuSn showed a considerable change in characteristics due to the high temperatures incurred during the bonding process. The process time for silver sintering is not critical as in the case of AuSn, where a longer process time would be detrimental to the joint. The under-bump metallization surface quality and thickness is also less critical for silver sinter. For assemblies with low pitch and small feature sizes, AuSn will still be the preferred choice due to the deposition methods making it possible to produce small feature sizes enabling bonding of miniature chips.

As the next step, the assemblies will be reliability tested to check the applicability for space environment.

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• ESTEC-ESA, Netherlands

[1] Datasheet TGF2023-2-01, '6 Watt Discrete Power GaN on SiC HEMT', www.qorvo.com, 2016.