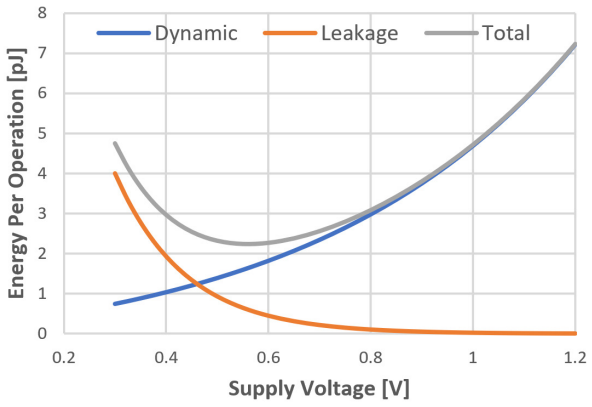
Beyond ultra-low-power

with body biasing and sub-threshold design

With the ongoing trend of more wireless connected devices, the requirements for extremely low power devices keep increasing. To meet those requirements, careful architecting of those devices is required, but also choosing the right building blocks is essential. In the design of ASICs, ultra-low power design methodologies such as body biasing and sub-threshold design have been known for already a long time, but have to date not made it into many products because it was deemed too cumbersome in the design phase and too risky to productize. CSEM has over the years built the expertise and developed robust design techniques and IP blocks to take away those hurdles.

Sub-threshold or near-threshold design

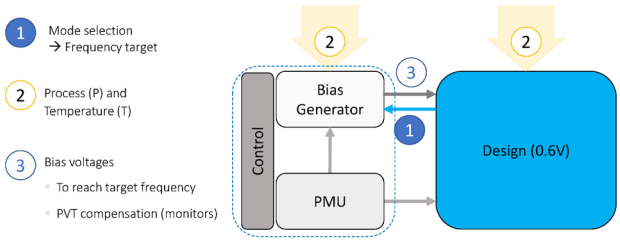
The total power consumption is a trade off between leakage and dynamic power.



The Minimum Energy Point (MEP) is for most CMOS processes in the sub-threshold or near-threshold region. The challenge is that in this region the process variation also has a much bigger influence, and therefore most digital designs have been done with higher voltages.

Adaptive body biasing

With adaptive body biasing it is possible to mitigate the challenges of the process variations at sub-threshold voltages. As such it is possible to save a very significant amount of energy and still be guaranteed to meet timing. Additionally, it is possible to adapt the body biasing to different use cases, and so in different modes to have either more performance or the lowest possible power.



CSEM's Adaptive body biasing and frequency scaling IP and design methodologies make it possible to design digital blocks with just the same robustness as for conventional designs, but with the benefits mentioned above.

UMC's C55DDC platform

An important demonstration of CSEM expertise is the partnership with UMC creating an ultra-low power IP platform targeting near/sub-threshold supply voltages in the UMC's 55nm DDC (Deeply Depleted Channel) technology. CSEM contributed essential parts such as :

- SRAM & standard cell design & characterization
- Body bias generators
- Adaptive body biasing and frequency scaling IP
- ADCs and DACs
- PMU (DCDC/LDO)

CSEM offers design services and consultancy for C55DDC, but also for other technologies such as Global Foundry 22FDX.

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