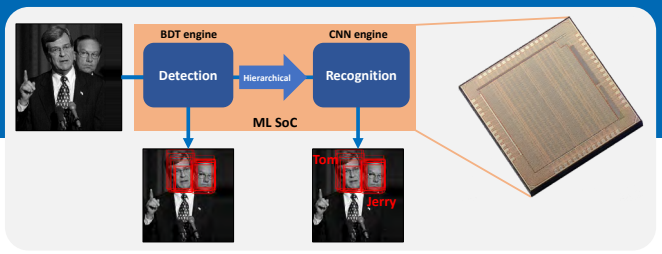
Machine Learning SoC



ULP system-on-chip with dual-engine ML acceleration

General description

This ultra-low power (ULP) machine learning system-on-chip (ML SoC) enables always-on image processing at the edge. The architecture allows efficiently integrating flexible binary decision tree (BDT) and convolutional neural network (CNN) algorithms along with a RISC-V-based icyflex-V microcontroller and more than 1 MB of memory. Miniaturized and power constrained IoT edge devices can benefit from the high computational efficiency and the complete on-chip end-to-end processing.

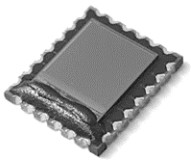
The ML accelerator subsystem and the icyflex-V core are also available as separate silicon IPs. CSEM IPs benefit from 20 years of experience in embedded computer vision, combining ULP ASICs and advanced ML algorithms.

Benefits

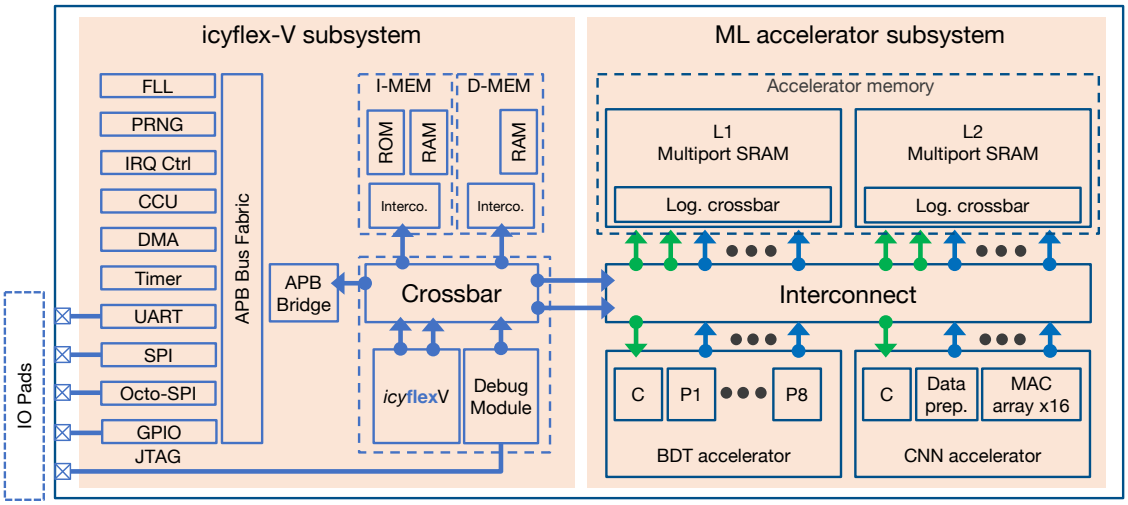
- Software stack included, with firmware examples for face detection (<2 mW for VGA)
- Support for standard ML flows (Caffe, TensorFlow, PyTorch)
- No need for external memory
- Energy-efficient Octo-SPI interface (particularly suited for a seamless integration with CSEM sub-mW HDR image sensor)
- Fully configurable IP: memory size, type of accelerator (can integrate BDT or CNN only)

Key specifications

- Optimized for hierarchical face detection and recognition, landmark localization, and eye-gaze tracking (<2 mW for VGA resolution)
- End-to-end inference for miniaturized systems
- The ML accelerator subsystem is compatible with APB and AHB bus for seamless integration with CSEM's icyflex-V or other microcontrollers
- Flexible dual-engine architecture accelerating both binary decision trees (BDT) for simple detection tasks and convolutional neural networks (CNN) for complex tasks
- Interleaved memory organization providing more than 20 GB/sec of bandwidth



e.g. CSEM ULP image sensor



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