A 1-1.5 mW Tx-Rx 2.45 GHz 200 kbit/s System-in-Package in Less than 13 mm³

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The WiserBAN EU FP7 project [1] coordinated by CSEM aims at the realization of an ultra-low-power miniaturized System-in-Package targeting wearable and implanted devices for healthcare, biomedical and lifestyle applications. The characterization of the first year [2] hardware results is reported below.

The dominant functional block, regarding the energy consumption as well as volume, because of associated passive components, is the radio transceiver. Classical architectures implementations are always a trade-off between overall volume and performances. This is especially the case concerning the energy consumption and particularly for the targeted applications for which all aspects are extremely constrained because of limited battery volume, i.e. capacity. In addition, the budget link needs to remain optimized because of very small antennas, disturbed and lossy propagation environments, etc. For this reasons, a novel architecture has been implemented in 65 nm standard CMOS technology, taking advantage of MEMS piezoelectric components, for further miniaturization (e.g. to get rid of quartz crystal), reduced energy consumption (e.g. to reduce star-up overhead) while conserving high-end radio performances (e.g. low-noise fine-step fully programmable frequency synthesis).

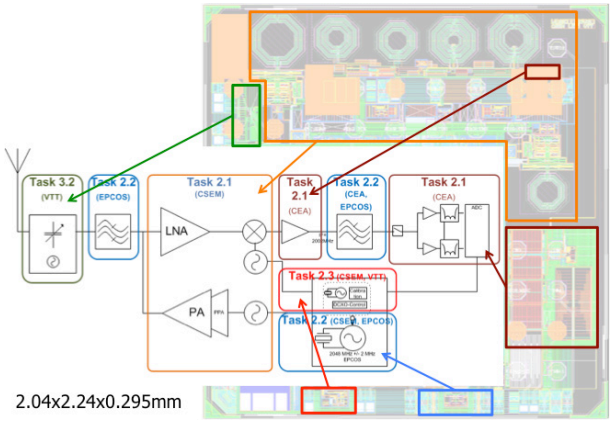

Figure 1: Radio transceiver architecture and associated layout

The radio transmitter architecture illustrated in the above Figure 1 profits from a 2 GHz BAW resonator and wide synthesizer bandwidth for direct digital modulation and very fast start-up (i.e. <5 µs), to reduce associated energy overhead (<30 nJ) and minimize energy consumption for short data packets (9 nJ/bit at 0 dBm 2 Mbit/s). For the targeted datarate of 200 kbit/s, the power consumption is close to 1 mW.

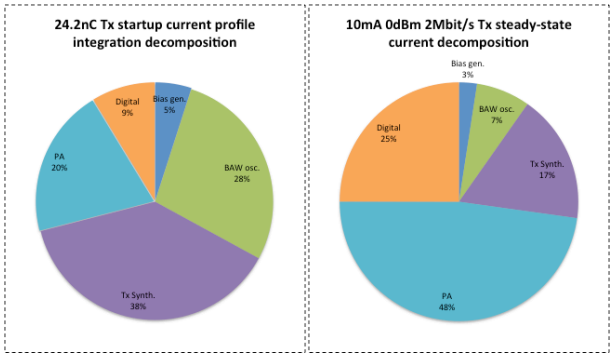

Figure 2: Transmitter start-up and steady state currents

The radio receiver architecture, illustrated in Figure 1, also profits from the fast synthesizer and a sub-sampling at high IF to also minimize the start-up overhead (<10 µs & <100 nJ), especially useful for channel sampling schemes. For the targeted datarate of 200 kbit/s, the power consumption is close to 1.5 mW.

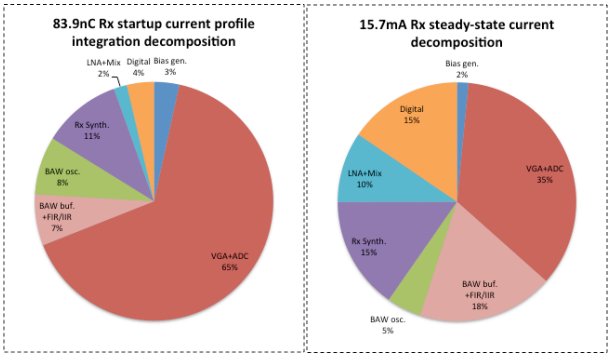

Figure 3: Receiver start-up and steady state currents

To address different application contexts, the architecture and digital baseband covers physical layers of 802.15.4 (250 kbit/s), Bluetooth LE (1 Mbit/s) and a 2 Mbit/s MSK proprietary mode.

The System-on-Chip also implements a CSEM-proprietary low-power (75 µA/V/MHz) DSP for control, protocol and processing, with 96 kB RAM, RTC, SPI, GPIOs, etc. and is implemented with all the passives into the thickness of a FR4 System-in-Package illustrated in Figure 4 below that will be reduced to below 13 mm³ with the use of 2nd generation resonators in Waver-Level-Chip-Scale-Package form.

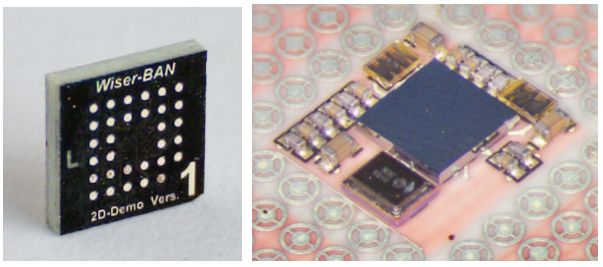

Figure 4: 4.25 x 4.25 x 0.77 mm system-in-package

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[1] WiserBAN: EU Project 257454 www.wiserban.eu

[2] "WiserBAN: A smart miniature low-power wireless microsystem for body area networks", CSEM Scientific and Technical Report (2011) 85