IntelliDUST—Intelligence in 3D Accelerometer Sensors at Zero-added Power Cost

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Sensors generate raw signals that need processing before providing value. With the advent of new generation of deep-ultra-low power sensors (μW consumption range), the consumption of processing algorithms is becoming dominant and therefore it is limiting for low-power applications. This work shows it is possible to provide the intelligent algorithmic layer without impacting the already negligible consumption of sensors by combining CSEM's algorithmic and ultra-low power know-how. The study is presented for 3D accelerometers sensors and activity tracking processing algorithms.

The power consumption of 3D accelerometers has been continuously decreasing over recent years from more than 100 µW (*e.g.*, ADXL345) to less than 4 µW (*e.g.*, ADXL362) and this trend is still on-going. On the contrary, related processing algorithms running on standard microcontrollers still consume in the order of 100 µW nowadays, impacting overwhelmingly the power budget.

The goal of this work is to bridge this gap for a particular case relevant to the market: physical activity tracking based on inertial sensors (*e.g.*, 3D accelerometers). The booming industry of wearables (*e.g.*, smartwatches, smart-textiles) where reduced consumption leads to extended autonomy and thus increased user comfort would greatly benefit from such results.

CSEM has a long history of algorithm design, development, and implementation in low-power wearable devices relying on inertial sensors. Among them, the following might be highlighted: activity profiling [1], kinetic [2] and gait [3] analysis, energy expenditure [4], fall detection [5] and swimming performance monitoring [6]. The ultimate goal is to add such intelligent algorithmic layers with negligible overall consumption overhead to turn a simple 3D accelerometer into a smart sensor. Five alternatives have been studied and are described below. Table 1 summarizes the results.

Table 1: Activity tracking algorithm consumption and flexibility.

#	Hardware	Supply	Algorithm	Sensor	Flexibility
1	CortexM0	1.8V	90 µW	4 µW	Yes
2	icyflex2	1.0V	16 µW	4 µW	Yes
3	Accelerator	1.0V	1 µW	4 µW	No
4	Accelerator	0.5V	0.1 µW	4 µW	No
5	icyflex2	0.5V	0.8 µW	4 µW	Yes

Option 1 is the reference design and uses an ARM's Cortex-M0 microcontroller embedded into a Nordic BLE transmitter (NRF51822) to run the activity tracking algorithm software. Power consumption is estimated to 90 µW. Option 2 uses CSEM's low-power icyflex2 microcontroller [7] implemented in standard 55 nm bulk technology (at 1 V nominal voltage). Power consumption is estimated to 16 µW and is still too high when compared to the 4 µW sensor consumption. Option 3 is to design a dedicated hardware accelerator for the activity tracking algorithm using the same standard 55 nm technology. Power consumption reduces to 1 µW, which is already lower than the sensor consumption. It could already be interesting depending on the application power budget. Option 4 is to go one step further for the dedicated hardware accelerator design and use sub-threshold voltage design on a specially tailored MIFS Deeply Depleted Channel (DDC [8]) 55 nm technology (at 0.5 V supply voltage). The power consumption is estimated to 0.1 µW, more than one order of magnitude lower than the sensor. Option 5 is based on the sub-threshold technology and conditions of option 4 but the algorithm is executed on an icyflex2 microcontroller [9]. In this case, running the algorithm draws 0.8 µW, similar to that of the dedicated hardware accelerator at nominal voltage, but with the advantage of having the flexibility of a microcontroller. The algorithm can thus be tailored to the application needs or refined during the product lifetime.

As expected, dedicated hardware accelerators show the lowest power for adding higher level intelligence such as activity tracking to a 3D accelerometer with up to 100-1000x power gain compared to the reference design, marginally impacting the sensor power budget. However, thanks to CSEM's know-how in sub-threshold design, comparable power levels are obtained when implementing the algorithm on an icyflex2 general purpose microcontroller, yielding the best of the power-flexibility trade-off.

[1] R. Delgado-Gonzalo, *et al*., "Learning a Physical Activity Classifier for a Low-power Embedded Wrist-located Device," IEEE BHI (2018).

[2] M. Bertschi, *et al*., "Accurate Walking and Running Speed Estimation Using Wrist Inertial Data," IEEE EMBC (2015).

[3] R. Delgado-Gonzalo, *et al*., "Real-time Gait Analysis with Accelerometer-based Smart Shoes," IEEE EMBC (2017).

[4] R. Delgado-Gonzalo, *et al*., "Human Energy Expenditure Models: Beyond State-of-the-art Commercialized Embedded Algorithms," DHM (2014).

[5] C. Moufawad el Achkar, *et al*., "Real-time Fall Detection Using Smartwatches," EU Falls Festival (2018).

[6] R. Delgado-Gonzalo, *et al*., "Real-time Monitoring of Swimming Performance," IEEE EMBC (2016).

[7] J.-L. Nagel, *et al*., "The icyflex2 Processor Architecture", CSEM Scientific and Technical Report (2009).

[8] K. Fujita, *et al*., "Advanced Channel Engineering Achieving Aggressive Reduction of VT variation for Ultra-low-power Applications," IEEE IEDM (2011).

[9] M. Pons, *et al*., "A 0.5V 2.5 µW/MHz Microcontroller with Analog-Assisted Adaptive Body Bias PVT Compensation with 3.13nW/kB SRAM Retention in 55 nm Deeply-Depleted Channel CMOS," IEEE CICC (2019).