Press release

CSEM and USJC team up to develop an ultra-low-power chip

Neuchatel, 10 August 2021 – After five years of joint R&D, CSEM and Japanese multinational United Semiconductor Japan Co., Ltd. (USJC)* have developed an ultra-low-power system-on-chip that can be used to run smartphones, tablets and other connected devices. Their technology probably delivers the best performance in the world when it comes to power consumption.

System-on-chips are the tiny powerhouses that make all kinds of connected devices – including smartphones and medical implants – possible. They alone contain all the main components of a computer, including memory, sensors and processors.

Circuit engineers are constantly looking for ways to lower the chips' power requirement in an effort to make them ever more compact, long-lasting and versatile. "That could mean, for example, keeping the power requirement constant between generations of devices, such as smartphones, which are the same size as the phones we used ten years ago but have 100 times more features. Or using a different kind of power supply, like a tiny solar panel, to run a device," says Stéphane Emery, head of system-on-chip research at CSEM.

Developing a complete integrated circuit

That search is what drove engineers at USJC, former Mie Fujitsu Semiconductor Limited (MIFS), to approach CSEM five years ago. They wanted to develop a chip that included all the components needed for their proprietary Deeply Depleted Channel (DDC) technology but that ran on very little power. The advantage of DDC systems is that they can operate at near- and sub-threshold voltages by minimizing a variety of factors, including transistor variation. CSEM engineers assisted with the design and assembly of the integrated-circuit components and helped come up with a method for reducing its power requirement as much as possible.

CSEM and USJC jointly developed the entire system hierarchy: the chip's base components, the memory capabilities that let it store data at very low voltages, and the functional blocks – the RISC-V processor, the Bluetooth radio that enables wireless connectivity and the converters that turn real-world signals into digital inputs.

Boosting efficiency and minimizing power leakage

The CSEM-designed processor employs a special method called Adaptive Body Biasing (ABB). This method allows it to operate efficiently in all modes – on, standby and off – while minimizing power leakage when the processor isn't running. It also delivers the best possible performance when the processor is active. "Many applications involve periods of time when the processor sits idle, waiting for an external event before it wakes up and processes information," says Emery. "ABB reduces the amount of power leakage during these periods. And it enables processors to operate in a highly efficient way when they do kick in."

Yoshie Keizaburo, a Senior Vice President at USJC, says: “By combining the world-class experience of CSEM in ultra-low power design with USJC’s unique DDC technology, the teams were able to demonstrate world-beating low-energy performance ideal for wearables and IoT.”

USJC * : Former Mie Fujitsu Semiconductor Limited (MIFS)

Additional information : Press kit

CSEM

Simon Gray
Head of Business Acquisition
Tel. +41 32 720 50 80
Mobile: +41 79 569 81 21
E-mail: simon.gray@csem.ch

CSEM - Media

Laure-Anne Pessina
Strategic Communication Manager
Tel. +41 32 720 5226
Mobile: +41 79 360 25 38
Email: laure-anne.pessina@csem.ch

About CSEM

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