icyflex-V RISC-V

A low-power RISC-V processor

CSEM is member of the RISC-V foundation (http://www.riscv.org) and provider of RISC-V hardware components.

The icy*flex*-V 32-bit processor core is based on the RV32IMC open-instruction set architecture (ISA) defined by the RISC-V foundation and, as such, is supported by standard state-of-the-art development tools (both open-source and proprietary). The 4-stage pipeline is optimized for power and area efficiency. Additional customizations are available on demand (e.g. RV32E area efficient implementation).

The icy*flex*-V core targets traditional micro-controller applications and is well suited for IoT, wearables and mixed signal applications.

The core IP comes along with various bus interconnect IP's and standard peripherals. For example, implementations relying on an embedded flash will benefit from an energy oriented cache architecture.

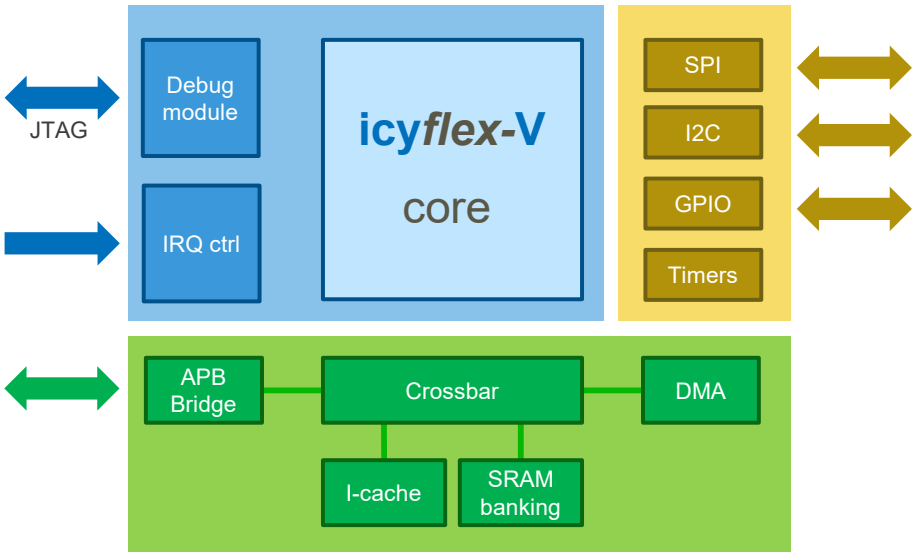
Features

- RISC-V RV32 instruction set:
  - I → full support
  - M → partial support: no hardware divider
  - C → full support
- Machine mode only
- 32 vectorized interrupts
- Standard debug as defined per RISC-V
- 3.06 CoreMark/MHz
- 1.35 DMIPS/MHz
- Gate count: 26 kgates

Implementation in TSMC 55 nm LP HVT

Please contact us for estimation in other process options

- Core only area : 0.056 mm^2
- Max. frequency (SS corner, 1.08 V, -40 °C) : 120 MHz
- Power consumption 18 uW/MHz
  (TT corner, 1.2 V, 25 °C)



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