Implementation and Benchmarking of RISC-V Microprocessors

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CSEM has evaluated two RISC-V microprocessor architectures which are freely available and suitable for integration on low-power System-On-Chips. Both RISC-V cores were synthesized and mapped to a Field-Programmable-Gate-Array (FPGA) and benchmarked using CoreMark. As a RISC-V Foundation member, CSEM complements its actual offer of low-power microprocessors for the industry with RISC-V cores.

RISC-V (pronounced “risk-five”) is a new instruction set architecture (ISA) originally developed for research and education at the University of California, Berkeley. It is now set to become a standard open architecture for industry implementations.

Figure 1: The RISC-V logo.

The RISC-V Foundation [1], a non-profit corporation controlled by its members, directs the future development and drives the adoption of the RISC-V ISA. CSEM is (together with numerous companies such as AMD, Google, HP, IBM, NVidia, NXP and Qualcomm) a registered member of the RISC-V Foundation.

The goal of RISC-V is to provide a completely open ISA that is freely available to academia and industry. The ISA avoids "over-architecting" for a particular microarchitecture style or implementation technology.

The base integer ISA is available for 32-bit, 64-bit or even 128-bit architectures. Standard ISA extensions exists e.g., for hardware multiplication and division; atomic instructions; IEEE-compliant floating-point arithmetic with single or double precision; compressed 16-bit instructions (to reduce code size).

In addition to supporting standard general-purpose software development, another goal of RISC-V is to provide a basis for non-standard extensions for custom instructions or application-specific hardware accelerators.

The University of California, Berkeley, not only provides and maintains a GNU based open-source toolchain (including compiler, standard-library, debugger and simulator), but also a configurable reference RISC-V system, the "Rocket Chip", available completely free as synthesizable RTL source-code [2].

The Rocket has a single-issue in-order 5-stage pipeline and its 64-bit core implements the RISC-V basic ISA and all standard extensions, including double-precision floating point arithmetic and compressed instructions.

In 2016, the ETH Zurich and the University of Bologna have together released an open-source RISC-V core called "RI5CY" as part of their Parallel Ultra-Low power processing Platform (PULPino) [3].

The RI5CY has a single-issue in-order 4-stage pipeline and implements the 32-bit base integer architecture, the compressed instructions extension and several proprietary ISA extensions such as: hardware loops, post-incrementing load and store instructions, SIMD and MAC operations.

At CSEM, we have used Xilinx Vivado to synthesize and map both RISC-V cores on a FPGA (Xilinx ZYNQ 7020) at 25 MHz. A low-cost FPGA development board "ZedBoard" was used to debug, assess and benchmark the cores.

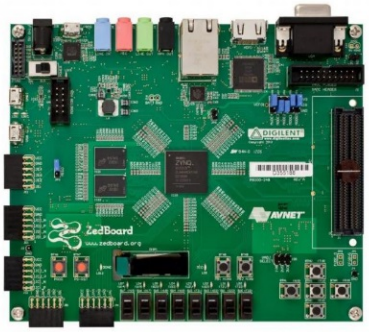

Figure 2: ZedBoard with a Xilinx ZYNQ 7020 FPGA.

When not taking into account the size of the optional floating point unit (FPU), the Rocket core is smaller, although it implements a 64-bit architecture and has a deeper pipeline.

The EEMBC CoreMark [4] is the leading industry-standard benchmark for CPU cores. CoreMark is capable of testing a processor’s basic pipeline structure, basic read/write, 32-bit integer and control operations. We have compiled the source-code (using gcc -O3) to benchmark the performance of both RISC-V FPGA implementations. Obviously, the RI5CY benefits clearly from its proprietary ISA extensions, while the Rocket's additional features (64-bit architecture and FPU) bring (as expected) no advantage for CoreMark.

Table 1: FPGA synthesis and benchmark results.

Core	Architecture	MHz	Size (cells, w/o FPU)	CoreMark /MHz
Rocket	Rocket Chip	25	6900	2.16
RI5CY	PULPino	25	9660	2.84

As RISC-V Foundation member, CSEM wants to provide RISC-V cores for the industry and complements its actual offer of low-power microprocessors. In this initial study, we have proven that these two freely available open-source cores are indeed ready to use. CSEM is working on architectural improvements, adding customized instructions and hardware accelerators, to integrate RISC-V cores in low-power System-On-Chip on real silicon (ASIC).

[1] https://riscv.org/risc-v-foundation

[2] https://github.com/riscv

[3] https://github.com/pulp-platform/pulpino

[4] http://www.eembc.org/coremark/index.php