A 0.5 V Near-threshold Microcontroller Robust over PVT Variations

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In this work, performed in close collaboration with Mie Fujitsu Semiconductor Limited (MIFS), specific libraries using a novel bulk biasing technique have been developed. To validate the concept, a circuit based on an icyflex2 processor has been integrated and characterized over PVT (Process, Voltage and Temperature) variations. The results demonstrate the advantage of the MIFS 55 nm DDC technology for low-power integrated circuits operated in the near threshold domain (0.5 V).

Ultra-Low Leakage (ULL) transistors available with MIFS DDC technology have been specifically engineered to operate at 0.5 V, with a reduced leakage current, so as to minimize the dynamic power consumption. This is achieved owing to a large body effect and a specific bulk doping profile, leading to improved matching. Working in the near threshold voltage region, rather than at a typical nominal voltage of 0.9 V, has two main negative consequences that need to be addressed: 1) the reduction of the speed of the transistor, and 2) the larger performance spread and mismatch among transistors.

After having taken into account various different trade-offs, such as speed, power, leakage, matching and tunability, a complete set of logic cells was designed using an optimally sized MOS transistor geometry. Having all transistors with the same dimensions yields a better matching with respect to their currents and hence control of their speed-over the entirety of bulk biasing voltage range.

Thanks to the wide current tuning capability of the DDC technology due to its high impedance bulk terminal, the decrease in speed and the performance variation between the different operating conditions can be partially compensated in a lower power way. The left hand side of Figure 1 shows that a factor 10'000 of transistor current variations between best (BC) and worst (WC) case PVT conditions is obtained at 0.5 V without compensation. With compensation (right hand side of Figure 1), the large variation is reduced to below a factor of two.
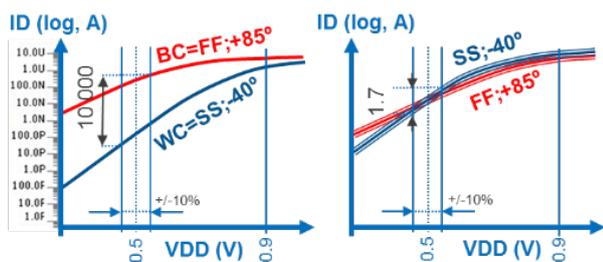

Figure 1: Transistor current variation for worst and best cases without (left) and with (right) the compensation mechanism.

A specifically designed voltage regulator continuously adapts the bulk bias to the PVT conditions; it allows, as shown in the right side of Figure 1, a reduction of the variation from an initial factor of 10'000 to less than a factor of 2. Moreover, by choosing the reference current (Iref), one can tune the transistor strength, hence the system speed.

Using the standard cells that were developed, a test vehicle circuit containing 50 different ring oscillators using most diverse types of cells as well as a 32-bit processor system was manufactured. The frequency measurements of compensated rings over various PVT conditions (Slow-SS, Fast-FF and Typical-TT) are shown in Figure 2, given Iref set for maximum speed and normalizing the values to the case of 0.5 V and 25°C.

Overall, the frequency variation is within +/-30% over PVT range of PVT conditions considered.
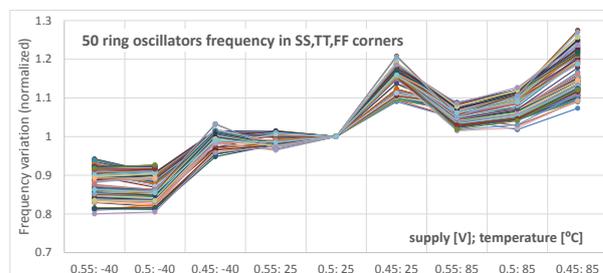

Figure 2: Normalized frequency of diverse rings measured over PVT.

Applying the same compensation methodology to the icyflex2 32-bit processor yields the results presented in Figure 3. Dashed lines show the maximum measured frequency for all extreme corners over the given temperature range [-40 ºC…125 ºC] and the range of supply voltages [0.45 V…0.55 V], at an Iref of 100 µA. Over the PVT conditions considered, a difference between the min and max frequency of only a factor of 2 was found. This is a drastic improvement compared to the 10 K variation of Figure 1.
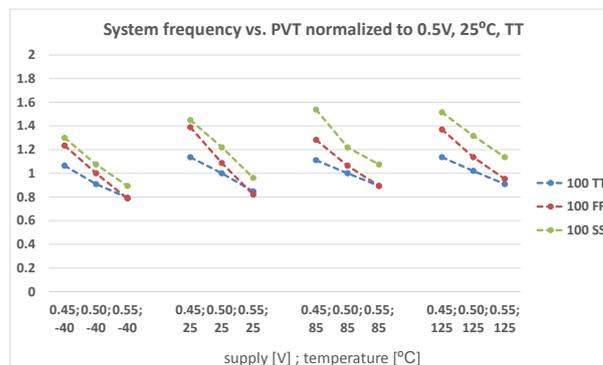

Figure 3: icyflex2 maximum frequencies in PVT with Iref=100 Ma.

These results demonstrate that Adaptive Bulk Biasing can successfully be applied to compensate for PVT variations of 0.5 V near-threshold logic circuits implemented with MIFS C55DDC technology while maintaining a good processor performance. Moreover, Bulk Biasing provides an additional knob allowing to tune the performance of the circuit at runtime, without changing the power supply; hence preserving low dynamic power consumption. This enables us to define several modes of operation, where speed and leakage current (fast mode, slow mode, retention) may be traded depending on the required overall performance. As such, MIFS C55DDC technology is found to be a very good process particularly suited to implement ULP wireless sensor nodes that are needed for the IoT era.