Image Sensor with Stacked Photodiode

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An image sensor with stacked amorphous photodiodes over the pixel has been developed. It offers 100% fill factor while freeing place in the pixel enabling either to reduce the pixel size or to increase the complexity of the in-pixel processing for dedicated applications.

Natural visual scenes have a very wide illumination dynamic range, making it difficult to render a good image quality in challenging illumination conditions. CSEM previously developed a time-to-saturation pixel with in-pixel digital memory offering an intra-scene dynamic range in excess of 120 dB without parameter adjustment. However, this high intra-scene dynamic range and ease-of-use have to be paid for in terms of fill factor. To remedy the low fill factor (~ 20%), one solution consists in depositing the photodiode on top of the pixel instead of being part of the pixel. This enables close to 100% fill factor and also the whole pixel area can be used for circuitry.

Taking advantage of CSEM's know-how and skills in the field of amorphous photovoltaic solar cells, we have deposited on top of non-passivated chips a layer stack of amorphous silicon (a-Si:H). In each pixel, the a-Si:H layer stack is connected to the pixel circuitry through the top metal layer, as illustrated in Figure 1. A layer of ITO (Indium Tin Oxide) deposited on top of the a-Si:H forming a transparent counter electrode. The ITO layer is subsequently removed from the pad areas by laser engraving. The remaining ITO serves as a mask for etching the a-Si:H. Finally, a gold pad is deposited on top of the ITO to enable it to be biased.

An existing CSEM image sensor test chip [1] with a pixel pitch of 14 µm has been modified to accommodate the a-Si:H layer. It contains pixels with n-well to p-substrate photodiodes with a fill factor of 20% and pixels with a-Si:H photodiodes, with 100% fill factor, with different metal contacting areas on the same chip for comparison purpose. Two types of junctions have been deposited: i-p and n-i-p.

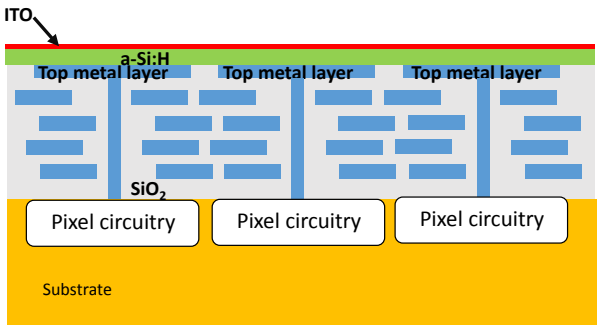

Figure 1: Image sensor module principle.

Figure 2 shows a microphotograph of the chip covered with a-Si:H and ITO. The different metal contacting areas are visible; the top part shows the unmodified sensor with in pixel photodiodes, the bottom part of the pixel array with 3×3 rectangles shows the 100% fill factor through stacked amorphous silicon.

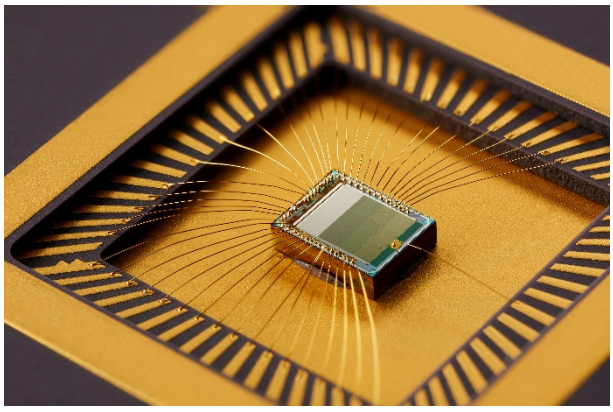

Figure 2: Microphotograph of the chip with top part of the chip unmodified and the lower part (3×3 square array) showing the amorphous photodiodes with 100% fill factor.

Figure 3 shows an image acquired with the test chip. It illustrates the difference of sensitivity between in-pixel n-well-substrate photodiodes and stacked a-Si:H photodiodes. The top part of the image is obtained with standard pixels with in-pixel n-well-p-substrate photodiodes, while the rest of the image is obtained with stacked a-Si:H photodiodes. The sensitivity is more than 6x higher with the stacked photodiodes compared to in-pixel photodiodes. The leakage current at room temperature is between 0.2 and 0.3 nA/cm^2 and does not vary by more than 3%/V as a function of the reverse bias applied.

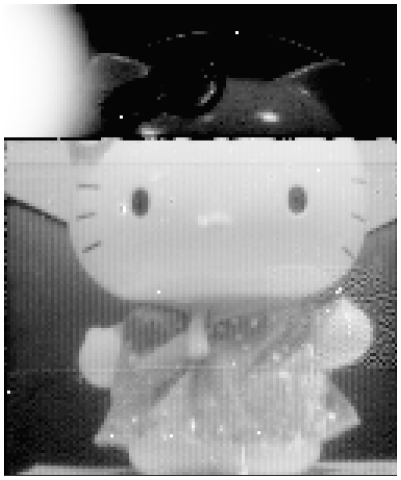

Figure 3: Sample image acquired with the test chip.

In addition to offering 100% fill factor, the proposed approach also enables electron imaging, such as in image intensifier systems based on a photocathode, vacuum imaging of particles, electron microscopy, beam imaging and X-ray applications.

[1] P. Heim, F. Kaess, P.-F. Rüedi, "High dynamic range versatile front-end for vision systems", CSEM Scientific & Technical Report (2007), 25.