A 500 µW, 0.5 V VCO and Fractional Divider for BTLE Robust over PVT Variations

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A low-power VCO and fractional divider robust with respect to process, voltage and temperature variations has been developed for IoT and energy harvesting applications. Integrated in a 55 nm deeply-depleted channel (DDC) technology, the body biasing feedback based circuit compensates the transistor drain-to-source IDS current and guarantees full functionality over three process corners (TT, SS and FF), at 0.5 V ± 10% supply voltage and over a temperature range between -40°C and 85°C.

Lowering the voltage is a promising solution to reduce the digital dynamic power consumption and extend the system lifetime of IoT and energy harvesting applications. The frequency synthesizer and, more specifically, the VCO and the fractional divider are power hungry blocks that can take advantage of the lower voltage to reduce transceiver power consumption. However, this strategy comes at a cost in terms of large transistor drain-to-source current (IDS) variability over process, voltage and temperature (PVT) variations due to its near/sub-threshold operation, making the design of these critical blocks more challenging.

This work proposes a 2.8 GHz VCO and a dynamic fractional frequency divider that is highly robust to PVT variations; made possible through the use of a body bias feedback technique. The proposed solution consumes 500 µW from a nominal 0.5 V supply voltage.

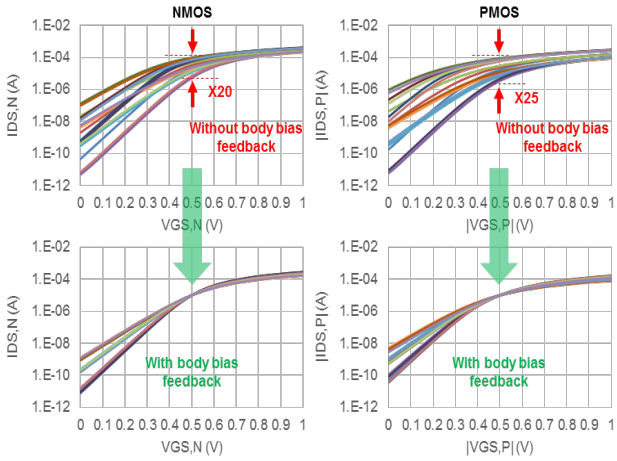

Figure 1: IDS vs VGS characteristic for an ULL NMOS and PMOS transistor with and without body bias feedback across PVT corners.

Figure 1 shows the IDS versus gate-to-source voltage (VGS) characteristic for ultra-low leakage (ULL) NMOS (left) and PMOS (right) transistors, with and without the proposed body bias feedback across PVT corners. When no bulk biasing is applied (VBS = 0 V), the current variation across PVT is increased as VGS is reduced. The proposed adaptive body feedback loop generates the required bulk voltage to enable the transistor to deliver a constant current independently from PVT variations. As a result, the 20 times PVT current dispersion observed at VGS = 0.5 V is compensated for a given 10 µA reference current (see Figure 1).

The circuit has been integrated using a 55 nm DDC CMOS technology from Mie Fujitsu Semiconductor. It is composed of a NMOS cross coupled VCO with a body feedback current control loop, a dynamic frequency divider (by four), a 5-stage cascaded 2/3 dual-modulus divider and a second order delta sigma mash modulator. Four bulk biasing sections composed of low, standard and high threshold voltage transistors are used among the VCO and divider chain in order to cover the large frequency range of operation. The layout of the proposed circuit is depicted in Figure 2.

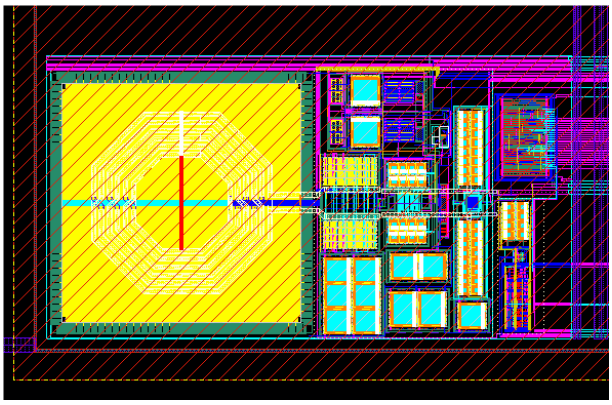

Figure 2: VCO and fractional frequency divider layout.

The results of simulations show full functionality of the circuit across three process corners (typical, slow and fast) from a 0.5 V supply, over a temperature range of -40 to 85°C. The VCO provides 10% frequency tuning centered at 2.8 GHz and consumes 400 µW of power. The dynamic frequency divider provides fractional frequency divisions in the range of 8 to 252, with a nominal power consumption of 100 µW.

This work has demonstrated how bulk biasing can be used for low voltage and low power applications covering a large range of frequencies, while offering more than 35% power reduction compared to the previous state-of-the-art [1,2,3].

• Mie Fujitsu Semiconductor Limited

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[2] A. Paidimarri, *et al.*, "A 0.68 V 0.68 mW 2.4 GHz PLL for ultra-low power RF systems," Proc. IEEE RFIC Radio Frequency Integrated Circuits Symposium (2015) 397.

[3] J. Silver, *et al.*, "An ultra-low-voltage all-digital PLL for energy harvesting applications," Proc. ESSCIRC European Solid-State Circuits Conf. (2014) 91.