Pre-Distortion Filter to increase Data Rate and/or Reduce Noise in Direct Frequency Synthesizer (G)FSK Modulators

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A pre-distortion filter implemented in the most recent versions of icyTRX is presented here. The filter reduces the PLL bandwidth of the direct frequency fractional frequency synthesizer modulator enabling the data rate to be increased and/or the adjacent noise/spurs to be reduced at the existing rate.

The new Bluetooth Low-Energy 5 specification adds a 2 Mbps data rate option to the existing 1 Mbps data rate. To address the higher data rate in the icyTRX direct frequency synthesis (G)FSK architecture, it is necessary to increase the Phase Lock Loop (PLL) bandwidth in proportion to the data rate in order to preserve the bandwidth of the modulating signal. This bandwidth, without calibration, must be oversized in order to ensure that there is sufficient margin to address the data rate when the following parameters are varied:

- The temperature.
- The frequency versus voltage gain of the voltage controlled oscillator (VCO).
- The silicon chip-to-chip variations (loop filter passives, bias currents, etc.).

The variation of these parameters acts to either reduce or increase the PLL bandwidth, depending on their values.

In a direct frequency synthesizer modulator, if the PLL bandwidth is too narrow compared to the bandwidth required by the data rate, the inter-symbol interference (ISI) is increased, which introduces more errors in the receiver. On the other hand, an over-sized PLL bandwidth results in increased phase noise and more parasitic spurs radiated in transmit (TX) mode because these unwanted signals are not as efficiently filtered by the PLL. An over-sized PLL bandwidth makes it therefore more difficult to comply with regulatory guidelines concerning e.g., adjacent channel power (ACP), as well as, some FCC rules.

The idea presented here is to use a simple solution that allows us to significantly reduce the PLL closed-loop bandwidth used in icyTRX in the TX mode for direct (G)FSK modulation. Specifically, a digital compensation filter is added in order to keep the data rate constant, while reducing the PLL bandwidth. The benefits of reducing the closed-loop PLL bandwidth with such a compensation filter are better ISI performance, reduced phase noise and improved spurs rejection outside the closed-loop bandwidth of the PLL.

In the direct frequency synthesis (G)FSK modulator architecture, the bandwidth of the modulation signal is determined by the following parameters:

- Phase frequency detector (PFD) phase gain.
- Charge-pump current gain versus phase.
- VCO frequency gain versus control voltage.
- Passive loop filter.
- The programmable divider with a division factor N.

Some of these parameters are readily determined, such as the division factor N and the phase gain of the PFD. But the charge-pump gain variation is mainly correlated to the bias current source variation, which is sensitive to the temperature if a bias current source proportional to the absolute temperature (PTAT) is used. Further, the VCO gain is sensitive to the tuning voltage settled by the PLL and also to the variation of fabrication parameters (process corners). The passive loop filter is programmable, but it is also sensitive to the process corners. The PLL frequency response in closed loop range – *i.e.* the range where the modulation signal is low-pass filtered in direct modulation principle – is fully defined by the previously mentioned parameters. There are no (or just a few) parameters that may be feely adjusted to change the shape of the frequency response of the modulated signal.

Our approach is to add a numerical "pre-distortion filter" in the digital path of the modulation signal that may be used to directly modulate the fractional frequency synthesizer via the ΣΔ. This provides a degree of freedom, which is necessary to adjust the initial "analog" closed-loop frequency response of the PLL e.g., to flatten the amplitude and the group delay frequency responses in the modulation signal path. The result is that the frequency response of the modulated signal is *different* than the "analog" PLL frequency response. The amplitude and phase (group delay) frequency responses are compensated via a pre-accentuation digital filter. Figure 1 shows the eye-diagram of a 1 Mbps (G)FSK signal without pre-distortion and Figure 2 shows the results with pre-distortion applied to the same PLL bandwidth.

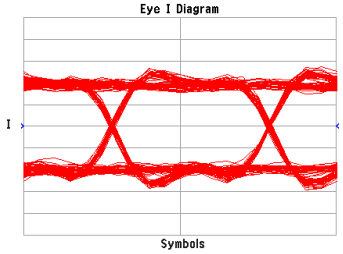

Figure 1: Eye-diagram without pre-distortion filter applied.

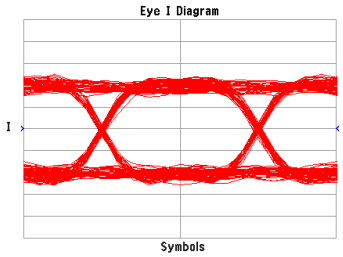

Figure 2: Eye-diagram with pre-distortion filter applied.

The advantage of the proposed pre-distortion filter in the path of the modulation signal is about 4 to 5 dB more with respect to the rejection of unwanted fractional/references spurs and phase noise outside of the PLL bandwidth. Put differently, this is equivalent to multiplying the (G)FSK data-rate by a factor of 1.6 to 1.8, while keeping the "analog" PLL bandwidth constant.