Library Design in a DDC Technology Optimized for Sub-threshold Regime

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In collaboration with Mie Fujitsu Semiconductor Limited (MIFS), CSEM has designed a standard cell library using MIFS Deeply Depleted Channel (DDC) 55 nm technology operating at sub-threshold voltage. Lowering the circuit supply voltage reduces the power consumption, while body bias tuning guarantees minimum speed degradation and allows a drastic reduction of the spread of performance across the different corners.

DDC technology

DDC transistors use a standard bulk silicon structure with a few additional processing steps improving their performance (Figure 1). The main advantages are the reduction of the local variation of threshold voltage (Vth) of transistors and the improved control of Vth by body biasing techniques [1]. Both features make the DDC transistor a perfect candidate for sub-threshold design where Vth variability implies a degradation and spread of performance that can reach up to 3 orders of magnitude when considering process, voltage and temperature variations (PVT).

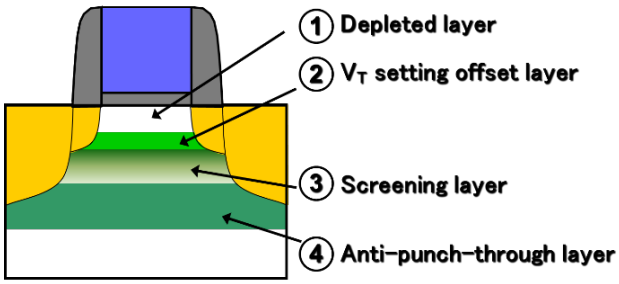

Figure 1: DDC transistor cross section layers.

Sub-threshold library with body bias control

A standard cell library optimized for 0.5 V operation was designed using DDC 55 nm Ultra-Low Leakage (ULL) transistors. The ULL option was chosen to reduce leakage (i.e. static consumption) in addition to achieving dynamic consumption reduction thanks to sub-threshold supply.

The library contains a reduced set of standard cells [2], including power management cells (i.e. level shifters, power switches, isolation cells, always-on-buffers). Transistor sizing was optimized so that the effect of body bias control is maximized allowing to compensate the full range of PVT variations (e.g. slow corner at 0.45 V and -40°C can achieve the same speed performance as fast corner at 0.55 V and 125°C by tuning the bias). All transistors in the library were therefore designed with a unique width and length; the channel length was slightly increased as compared to a nominal voltage library and transistor fingers were used for different drive strengths.

An adaptive body bias control circuit generates P and N well bias voltages depending on PVT conditions and on a given circuit operation mode (e.g. fast, medium or slow modes). Alternatively, maximum reverse body bias (increasing Vth of transistors) can be applied in sleep mode to minimize leakage.

Test vehicle circuit simulations

An 8 bit multiplier was used as a test vehicle for the standard cell library evaluation. The placed-and-routed layout was simulated at SPICE-level under different biases and PVT conditions. The simulation results are illustrated in Figure 2.

Performance at 0.9 V without bias control exhibits a spread of 3.2x and a maximum speed of the circuit of 74.5 MHz (the worst case determines the actual speed). At 0.5 V without bias control, the performance spread is 109x which results in unacceptable variation and also in very poor performance (0.7 MHz). Taking advantage of DDC bias control capability, the performance spread is reduced to 1.4x, 1.3x and 1.5x for fast, medium and slow modes (determined by the bias) respectively, which are smaller than the 3.2x spread observed at 0.9 V. At 0.5 V and fast mode, the maximum speed reaches 60.8 MHz, i.e. only 20 % less than the speed achieved at 0.9 V.

Regarding power consumption under typical conditions, the leakage power in sleep mode at 0.5 V is as little as 1.8 nW. Dynamic consumption is reduced by a factor of 3.4x (93.3 fJ/cycle versus 319.5 fJ/cycle) for 0.5 V in fast mode compared to 0.9 V operation.

Conclusion

Combining MIFS DDC technology and CSEM sub-threshold experience, we have developed a digital library allowing minimum degradation and spread of performance when operating at low supply voltage thanks to body bias control. Circuit consumption is also reduced by a factor better than 3x.

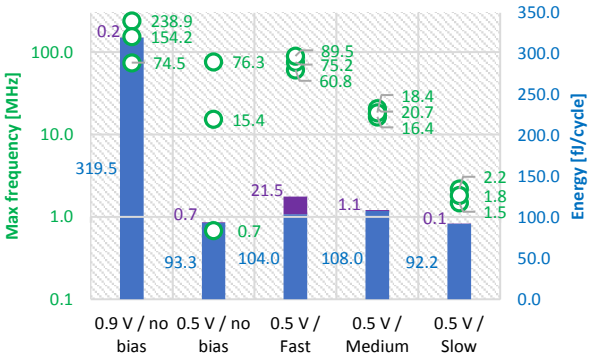

Figure 2: Multiplier maximum frequency and energy using sub-threshold DDC library. Best, typical and worst frequencies in the full range of PVT (green circles) show the performance spread. The bars indicate the dynamic (blue) and the static energy (violet).

• Mie Fujitsu Semiconductor Limited

[1] K. Fujita, *et al.*, "Advanced channel engineering achieving aggressive reduction of VT variation for ultra-low-power applications", IEDM IEEE International Electron Devices Meeting (2011) 32.3.1.

[2] M. Pons Solé, *et al.*, "Ultra low power standard cell design using planar bulk CMOS in subthreshold operation," PATMOS International Workshop on Power and Timing Modeling, Optimization and Simulation (2013) 9.