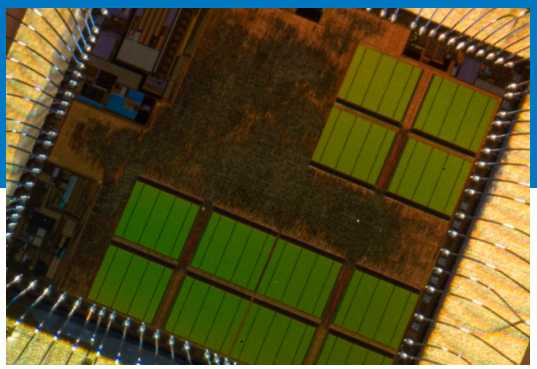


Ultra low-power icy*flex*® processors

icy*flex*®

Based on its long standing expertise in ultra low power processors for the Swiss watch industry, CSEM now offers three architectures in its icyflex family of ultra low-power processors:

- icy*flex2* for control type applications with power consumptions as low as 6 µW/MHz
- icy*flex1* for a mix of control and DSP-type applications
- icy*flex4* for a scalable architecture capable of some control and massive parallelism for DSP-type applications

Customizable architectures

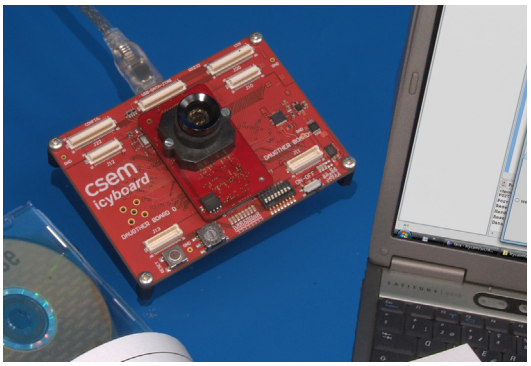
All 3 processors are available as VHDL soft blocks with multiple parameters (bus widths, stack size, optional blocks) so you only integrate the part of the processor you use.

Configurable architectures

The processors can be configured at run time to add new addressing modes and new instructions to reduce the number of cycles for individual algorithms.

High parallelism

The processors feature powerful datapaths (up to 36 MAC) and high bandwidth to registers and memory for maximum throughput per instruction, or clock cycle.



Software and hardware development kits available

Software development kit (SDK)

World-class GNU tool suite (compiler, assembler, debugger, cycle accurate instruction set simulator, ...) with plugin for the Eclipse IDE.

Hardware development kit (HDK)

Plug-and-play motherboard for development on System-on-Chip (SoC) and on FPGA to reduce time to market.

Quality

The processors are designed for testability and support On-Chip-Debug through a JTAG interface. Silicon proven.

Processor	icy*flex2*	icy*flex1*	icy*flex4*
Ultra low power	6 µW/MHz (65 nm LP)	120 µW/MHz (180 nm G)	150 µW/MHz (65 nm LP)
Powerful datapath	1 MULT, 1 ALU, 1 SHIFT	2 MULT, 2 ALU, 2 ACC, 2 SHIFT	4 + 4 VPS* MULT+ACC
Instruction width	32 bits (2 sub instr.)	32 bits (2 sub instr.)	64 bits (3 sub instr.)
Register data width	16 and 32 bits	16, 32 and 64 bits	16, 32 and 64 bits
Pipeline depth	5 stages	3 stages	5-8 stages
Max ops/instruction	6	16	33 + 31 VPS*
Data mem. bandwidth bytes/cycle	4	16 **	16 VPS **
Silicon area mm^2	0.05 (65 nm LP)	1.75 (180 nm G)	0.19 + 0.13 VPS* (65 nm LP)

**) VPS = Vector Processing Slices **) customizable*

Customer benefits

- High performance processors with best in class energy efficiency
- World-class environment for software development (GNU and Eclipse)

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