Press release – CSEM SA and Mie Fujitsu Semiconductor Ltd

Mie Fujitsu Semiconductor and CSEM join forces to develop ULP solutions for next-generation IOT devices.

Combining Deeply Depleted Channel and near / sub-threshold technologies to reduce energy

Neuchâtel (CH) and Yokohama (JP), 21 April 2016 – Mie Fujitsu Semiconductor Ltd (MIFS) and CSEM have penned a joint development agreement to cooperate in the development of Deeply Depleted Channel ("DDC") and near/sub-threshold technologies for the IOT/Wearables market. The agreement encompasses the development of ultra-low voltage, ultra-low power standard cell libraries, power management cells and memories as well as the development of a representative qualification vehicle to showcase the technology, and will include cross-licensing of related IP.

For wearable and IOT devices superior energy efficiency is crucial: the conflicting requirements of increased miniaturization along with longer battery life mean that standard CMOS technologies are reaching their limits and that new solutions are urgently needed. Since the power consumption of digital circuits is proportional to the square of the supply voltage, low voltage operation is the best hope for significant improvements while maintaining NRE costs in check.

Develop a best-in-class Extreme-Low Power platform

MIFS' Deeply Depleted Channel (DDC) technology enables fabrication of extremely-low-leakage transistors operating at supply voltages (Vdd) below 0.5V to obtain maximum power efficiency. DDC offers a better Vt mismatch & spread than conventional CMOS, allowing lower Vdd with minimum degradation of performance. Applying DDC to 40/55nm CMOS along with mixed signal/RF and embedded NVM allows cost-effective and highly integrated analog and RF SoCs for IoT /wearable platforms. MIFS has now joined forces with CSEM, with their long design experience in low-voltage, low-power integrated circuits, to develop an ultra-low power IP platform targeting near/sub-threshold supply voltages in the MIFS DDC technology. The goal is to develop a best-in-class Extreme-Low Power (ELP) platform with the associated ecosystem to enable chip designs for energy-critical wearable and IOT devices.

A win-win alliance

"MIFS DDC technology offers best-in-class low voltage and low leakage operation. By working with CSEM we will be able to develop an ecosystem to make the benefits of this technology available widely to our partners", says Masahiro Chijiiwa, Director of MIFS and Corporate Senior VP.

Alain-Serge Porret, CSEM's Vice President of ultra-low-power integrated systems, adds "The partnership with MIFS is fully aligned with CSEM's long-standing commitment to ULP design. We are thrilled to soon be able to add DDC-based IPs to our portfolio of solutions, allowing us to reinforce our offer of ultra-low power design services & IPs".

The development will be performed in close direct collaboration between process engineers, library specialists and ULP design experts, both in Japan and Europe, in order to unleash the full potential of the new platform, which is expected to be available for limited release in Q4 2016.

About CSEM

CSEM—technologies that make the difference

CSEM, founded in 1984, is a research and development center (public-private partnership) specializing in microtechnology, nanotechnology, microelectronics, system engineering, photovoltaics and communications technologies. Around 450 highly qualified specialists from various scientific and technical disciplines work for CSEM in Neuchâtel, Zurich, Muttenz, Alpnach, and Landquart.

Further information is available at www.csem.ch

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About Fujitsu

Mie Fujitsu Semiconductor is a pure-play foundry company based on 300mm wafer manufacturing facilities located in Kuwana City, Mie, Japan. Headquartered in Yokohama, it was established as a subsidiary of Fujitsu Semiconductor Limited on December 1, 2014. UMC became its minority shareholder in March, 2015. Mie Fujitsu Semiconductor provides high-quality technology and services, with wide-ranging expertise focusing on Ultra-Low-Power, Non-Volatile Memory and RF Technology.

For more information, please see: http://www.fujitsu.com/jp/mifs/en/

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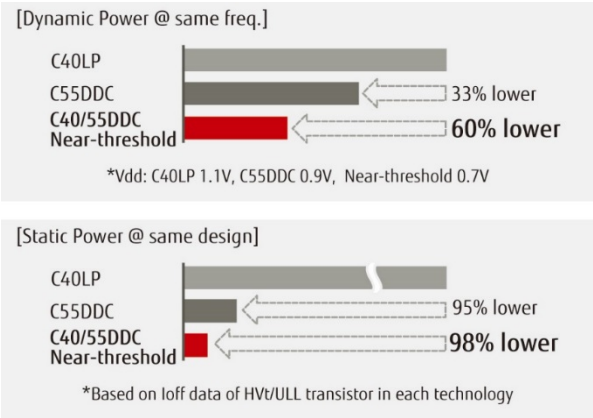
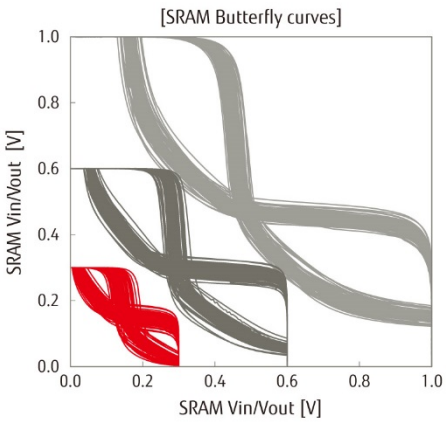
Appendix



DDC and a lower operating voltage enable significant total power reduction.



DDC enables an extremely low Vdd operation for SRAM: