An Off-chip Capacitor-free LDO with Fast Transient Response

J. Deng, P.-F. Rüedi, C. Monneron, P. Persechini

A LDO has been implemented for achieving good line and load regulation, fast transient reaction to large load current and supply voltage step, good noise and PSRR performances without off-chip capacitor.

The regulator is a linear low-dropout regulator (LDO), providing 1.2 V output voltage with a load current capability up to 100 mA with an input voltage range from 1.6 V to 5.5 V. It is designed for security applications, presenting the following features:

- Capability of driving either on-chip or off-chip blocking capacitor
- Fast reaction (meaning <50 mV output voltage drop in nominal case) to a large load current step (i.e. ±10 mA in 2 ns) or a large supply voltage step (i.e. ±0.5 V in 2 ns)
- Good line regulation and load regulation
- Good noise and PSRR performances

The conventional regulator structure is not capable of meeting the above requirements without a large off-chip capacitor. However, due to packaging constraints, no external capacitor can be accommodated. Thus, only on-chip blocking capacitor can be used. Stability and fast transient reaction are the two major challenges of this LDO.

The LDO structure is shown in Figure 1, implemented basing on a modified nested structure with zero-pole cancellation technique (indicated in Figure 2):

- Indirect feedback of the miller capacitor C_1 is to generate the dominant pole (p_1), as well a LHP (Left Hand Plane) zero (z_1)
- C_2 together with CG_2 is to fine adjust the position of z_1
- C_3 is optional, to reduce the Q factor of the conjugate complex pole pair, p_4&p_5
- A low impedance node, marked as "A" in Figure 1, is available for adding the “Transient Enhancement” block to improve the transient performance when a large load current step or a large supply voltage step occurs

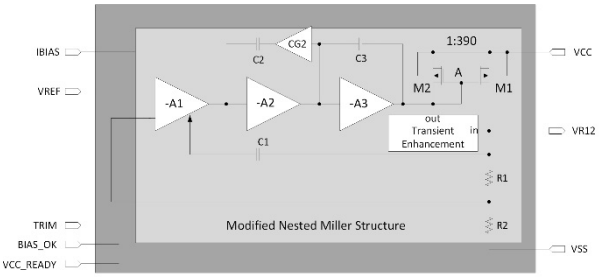

Figure 1: LDO block diagram.

The stability is achieved with zero-pole cancellation for the specified on-chip capacitor range, as shown in Figure 2. The pole of "p_2" is located at the LDO output, while the "p_3" pole is due to the C_{gs} of the output transistors "M1". Depending on the load current and the load capacitor, "p_2" shifts along the real-axis. The zero of "z_1" is carefully positioned so that the phase margin >50° is achieved under all conditions.

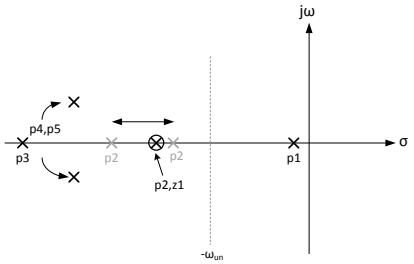

Figure 2: Zero-pole cancellation.

The GBWP of the LDO is about 50 kHz, which is not sufficient to achieve the required transient reaction against fast load current step or supply voltage step. The “Transient Enhancement” circuit is therefore introduced to improve the transient performance. The block diagram is presented in Figure 3.

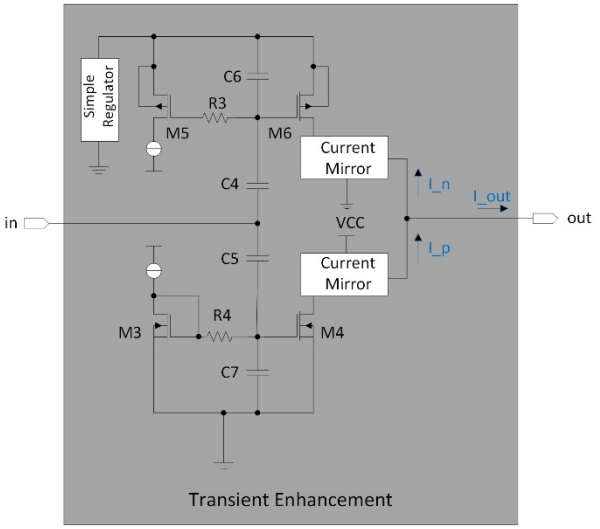

Figure 3: Transient enhancement block diagram.

The table below shows a summary of the LDO performances.

Technology	90 nm CMOS
Operation temperature	0°C to 105°C
Supply voltage	1.6 V to 5.5 V
Load capacitor	10 nF to 40 nF
Load current	0 mA to 100 mA
Step current	upto ±10 mA
Step supply voltage	upto ±0.5 V
Line regulation	<50 mV/V
Load regulation	<0.5 mV/mA
Integrated noise	<275 uV from 10 to 100 kHz
PSRR	>30 dB @ 1<freq<100 kHz >12 dB @ 100 k<freq<1 MHz
Current consumption	<0.5%*I_{load} + 0.25 mA
Area	0.2 mm^2 (excluding blocking capacitor)