Robust and Accurate Clock Synchronization for Wireless Sensor Networks

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Precise timing information is a key factor in computing and networking for applications that require a precise mapping of collected sensor data with the time at which the events were sensed. Clock synchronization is the process of ensuring that physically distributed nodes of a network have a common notion of time, despite the timing uncertainties (such as clock drifts, propagation delays, time-stamping mechanisms) from the transmitter to the receiver. Thanks to good models, it is possible to obtain accurate and also robust clock synchronization in practical settings.

Previous research or R&D activities on clock synchronization developed on top of the WiseMAC protocol has shown promising results. These have been further improved by removing the sources of uncertainty and better modelling of the variations.

When synchronizing clocks, timing uncertainties can degrade accuracy. Various different sources of uncertainty can be identified.

Time stamping is one of them. To reduce the timing uncertainty that it causes, time-stamping of the message is done at the physical layer instead of the MAC layer using the time capture capability of the used micro-controller (MSP430F5438A) to time-stamp radio transceiver interrupts. This removes most of the timing uncertainties due to the higher layers.

Propagation delay is a second source. The uncertainty is highly implementation dependent (IC, bit rate, modulation, event, etc.). We measured a CC1125 radio operating at 50 kbps every 5 seconds during 18 minutes and the results of the test showed that (Figure 1):

- The delay does not show a meaningful dependence on time
- It does not vary significantly. The maximum and minimum recorded values do not differ by more than 6.6 µs.
- The value of 81.5 µs (± 4 µs) can be safely taken as a constant delay value
- Other tests using similar hardware platforms have shown that the communication delay shows similar behaviour at different bit rates

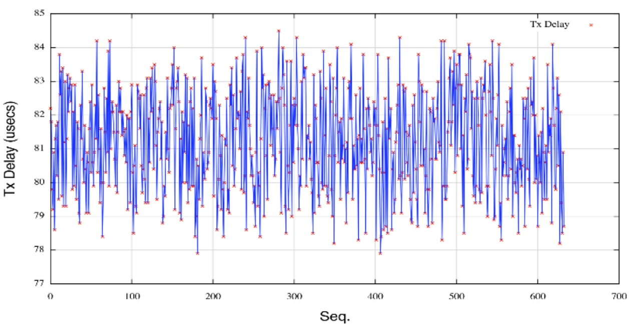

Figure 1: Transmission delay.

The Sink node inserts its clock value, with a granularity of 30.5 µs, into a special flooded clock synchronisation message. The reason of this value is that in the current hardware implementation of the nodes, the crystal oscillator has a frequency of 32768 Hz and, consequently, its granularity is of 30.5 µs.

Upon reception of a clock synchronization message, a node stamps the message and estimates the corrections that should be applied to the clock. These corrections are applied in such a way that local clock monotonously increases.

In order to validate the accuracy of the CSEM Clock Synchronization Protocol, several experiments were performed. One of the experiments consisted of a Sink and a node placed in a room with ambient temperature. The Sink sent a Clock Synchronization Message every 10 minutes. The experiment ran for 3 hours and the measured clock error was found to be less than 150 µs (Figure 2).

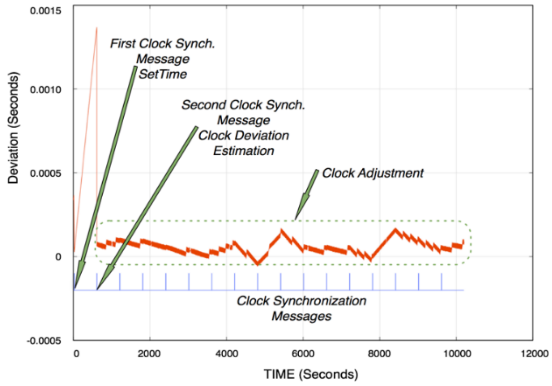

Figure 2: Clock adjustments under ambient temperature conditions.

A second experiment was performed in which a perturbation was introduced. This perturbation consisted of a cooling spray that was applied to the node after the fourth clock synchronization message. The clock deviation at that moment was about 1.3 ms, but three synchronization messages later, the measured clock deviation was again around 100 µs (Figure 3).

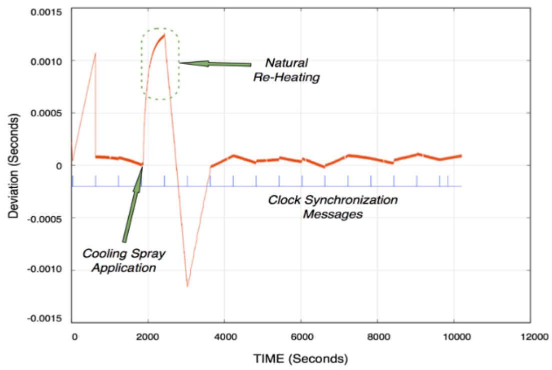

Figure 3: Clock adjustments under variable temperature conditions.

The experiments have shown that our protocol provides sub-millisecond accuracy with very little traffic even in the presence of severe temperature variations (shadow to light for instance). This does not degrade significantly with the number of hops.