Improving 55 nm Technology System-on-chip Functionality through In-house focused Ion Beam Corrections

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Debugging of disruptive elements in chip design is a regular process in order to obtain a fully functional chip. During the debugging of the chips designed by CSEM for prosthetic hand control in the DeTOP project, it was necessary to disconnect certain capacitive elements to remove problems associated with overconsumption of power without harming the system. To this end, Focused Ion Beam (FIB) was employed by using a focused Ga-ion beam, metallic connects at a precise depth were milled locally resulting in the disconnection of the disruptive capacitive elements. As a result, the corrected chip design was fully functional and was integrated into an ASIC for the demonstration of the prosthetic hand.

In the framework of the DeTOP project [1] we designed a 55 nm technology system on chip (see Figure 1) which addresses the recovery of hand function after amputation. The system on chip includes an electromyography (EMG) analog front end with an integrated 32b RISC core for prosthetic control [2]. However, we found an overconsumption issue, creating a noisy supply that was limiting its functionality. Currents in the order of 100 mA were drawn which were one order of magnitude bigger than expected. Design debug led to the identification of the misconnection in the supply network of the analog front-end block. It was required to disconnect already integrated capacitive elements without harming the functionality of the rest of the chip.

In order to achieve this, CSEM in-house Dual Beam FIB Thermo Fischer SCIOS 2 was used. A highly focused Ga-ion beam is used to remove material, resulting in extremely localized 'milling'. From the chip design, the metallic connects supplying power to the defective elements were identified, and areas were localized that would allow for the FIB milling to reach these layers without affecting any other elements. The FIB was operated with a 30 kV acceleration and beam currents of 3nA-5nA were used. By controlling the time for each milling operation, the depth of the milling process was controlled (which was critical for the 55 nm technology of the chip). Following each cut, the cross section was observed using a Scanning Electron Microscope (SEM) to verify the layers disconnected by the milling process (see Figure 2). For each chip, 14 cuts were undertaken. 6 chips were corrected.

After FIB correction, supply current was then measured again on the 6 chips and no overconsumption remained for 5 of them, allowing for fully functional design. The 6th chip was damaged during FIB, reaching 83.3% yield, which is high for this 55 nm technology considering the number of cuts performed.

Thanks to the FIB correction we were then able to control a prosthetic hand using EMG signals sensed on our arm [3] (see Figure 3). EMG signals are first used to train the prosthetic hand applying a pattern recognition algorithm. Once training is complete, the EMG signals that are sensed by CSEM ASIC control directly the prosthetic hand movements (the hand movements are reproduced by the prosthetic hand).

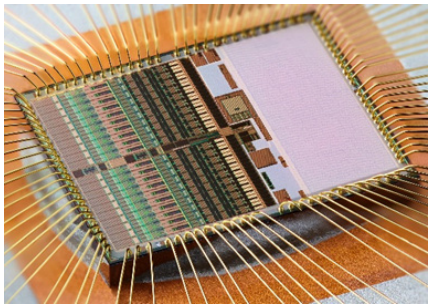

Figure 1: DeTOP system on chip micro-photograph (3 x 3.7 mm^2).

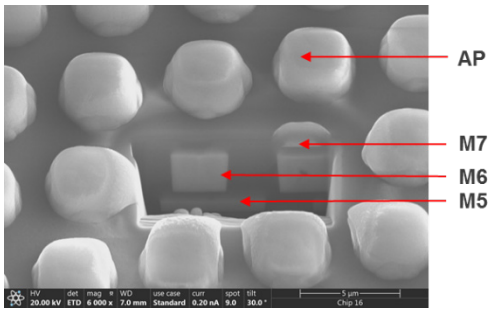

Figure 2: Cross section from FIB showing precise milling up to metal M5 layer while only touching inactive M6 and M7 layers.

Figure 3: Prosthetic hand control using DeTOP system on chip (CSEM ASIC).

[1] DeTOP project: European Commission under the Horizon 2020 Framework Programme for Research and Innovation (LEIT ICT 24 2015, GA #687905). http://www.detop-project.eu/

[2] M. Pons, *et al.*, "A 20 Channel EMG SoC with an Integrated 32b RISC Core for Real-Time Wireless Prosthetic Control," IEEE European Solid State Circuits Conference (ESSCIRC), Krakow, Poland (Sept. 2019).

[3] Video "DeTOP – CSEM: Miniaturised low-power ExG sensing front end ASIC for prosthetic applications", https://youtu.be/7PtQfvcDbCY