A Frequency Synthesizer for Ultra-low Phase Noise Multi-clock Generation

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The project Pheros focuses on the development of an integrated 2.7 GHz ultra-low phase-noise Phase-Locked Loop (PLL) frequency synthesizer with an up to 2.7 GHz programmable multi-clock generator for low-jitter and high-speed time-based applications.

The continuous Complementary Metal-Oxide-Semiconductor (CMOS) technology scaling has allowed for the development of high-speed communication modules such as Analog-to-Digital Converters (ADC). With the operating frequency of such devices nowadays reaching up to the gigahertz range, clock jitter has become the dominant source of sampling noise, increasingly driving sampling noise optimization.

Pheros has focused on the design of an ultra-low phase noise Radio Frequency (RF) Phase-Locked Loop (PLL). Illustrated in Figure 1 is the simplified block diagram of the proposed analog PLL. It uses a 54MHz crystal oscillator (XO) reference, an integer-N loop frequency divider, a Phase-Frequency Detector (PFD), a Charge Pump (CHP), a loop filter and a Voltage-Controlled Oscillator (VCO) operating in the range of 2.41 to 2.72 GHz. The core of the circuit, including the digital circuitry, is supplied from a 1.1 V source, while the XO is powered at 2.5 V. The proposed circuit uses a versatile programmable frequency divider in order to extend the user application domain. It provides divide-by-2 and divide-by-5 clocks with tunable duty cycle and phase shift. The VCO and the XO clocks are also accessible. Alternatively, an optional external clock allows the circuit to be driven by an external source, which may be required in multi-chip synchronized systems, where a single master chip can be used to drive the others, or where it may be convenient to reduce the component count by sharing a common XO.

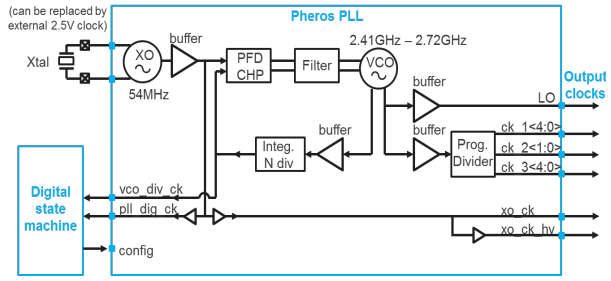

Figure 1: Block diagram of the proposed ultra-low phase-noise PLL.

As in any other conventional analog PLL's, the noise contributions of the crystal reference, the frequency divider, the PFD and the CHP are filtered by a low-pass transfer function as seen from the output clocks; whereas, the VCO phase noise is high-pass filtered. As a result, the in-band phase noise is dominated by the reference clock, and the high-frequency phase noise by the VCO. Optimization of the XO and VCO phase noise is challenging. It is mainly composed by a flicker noise component generated by the up conversion of the 1/f noise of the active devices around the carrier and a thermal noise component induced by the losses on the oscillator's tank. Hence, the flicker noise contribution was reduced by increasing the active transistor area, while the thermal noise component was minimized by regulating the oscillation to maximize the amplitude within the safe operating area of the devices.

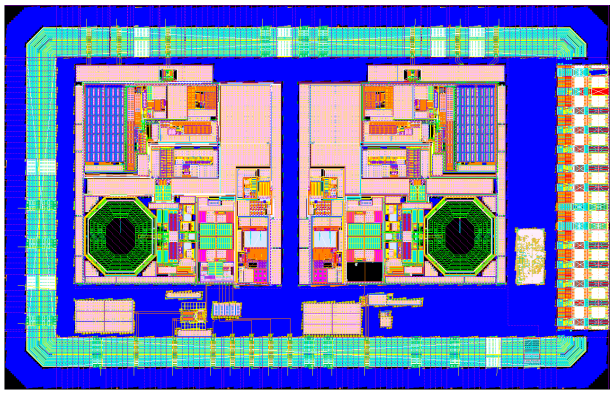

Figure 2: Layout view of the test circuit.

Figure 2 presents the layout view of the test circuit. The 1.26 mm x 2 mm circuit was integrated in a low power RF 40 nm TSMC technology. The circuit implements two symmetrical cores for test purposes with a core active area of 675 µm x 720 µm. The core PLL consumes 11 mA from a 1.1 V supply, while the XO current consumption is 0.45 mA from a 2.5 V supply. The results of measurements show a 100x XO phase noise improvement (20 dB) with respect to our previous in-house low power PLL reference and an 8x enhancement (9 dB) relative to the VCO. With -132 and -152 dBc/Hz at 1 kHz and 1 MHz offsets respectively, the 54 MHz XTAL oscillator has a Figure-Of-Merit (FOM) of -226 and -186, respectively.

Compared to the previous SOTA, very few circuits integrate the reference clock with the PLL [1,2]. Instead, they rely on external sources to achieve very good phase noise and jitter performance, hindering fair comparisons by obscuring the additional costs, integration complexity and power consumption of such solutions. Notably, 2019 reference [3], from the most reportable conference, presents only similar performance to Pheros, thereby demonstrating the excellent cutting-edge performance of the high-frequency time-reference, allowing us to further extend the operating frequency and resolution of the ADC's.

[1] Sharma, *et al.*, "A Dividerless Reference-Sampling RF PLL with - 53.5dB Jitter FOM and <-67dBc Reference Spurs", ISSCC (2018).

[2] X. Yang, *et al.* "-246dB Jitter-FoM 2.4GHz Calibration-Free Ring-Oscillator PLL Achieving 9% Jitter Variation over PVT", ISSCC (2019).

[3] Song, *et al.* "A Fractional-N Synthesizer with 110fsrms Jitter and a reference Quadrupler for Wideband 802.11ax", ISSCC (2019).