Standard Cell Library for Sub-Threshold Operation

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The use of MOS transistors operating in the sub-threshold region to design integrated circuits is a promising technique that will allow the development of future ultra-low power applications by reducing the required supply voltage and the power consumption. This motivates the development of new methodologies to generate standard cell libraries that can work in sub-threshold operations.

Low-power applications (such as wireless sensor networks, watches or RFID) are always demanding solutions to lower the power consumption and to support additional features. One possibility is to reduce the supply voltage (Vdd) of the circuit. When Vdd is lower than the threshold voltage of the transistors (Vt), the transistors are in sub-threshold operation and the power consumption is drastically reduced. However, ensuring the correct operation of sub-threshold designs is challenging as the ratio between active (Ion) and leakage (Ioff) currents is reduced. CSEM has proposed a methodology to adapt existing standard cell libraries for sub-threshold design.[1]

Objectives

Two major benefits can be achieved with sub-threshold design:

- Power budget reduction: Dynamic (Pdyn) and static (Pstat) power both depend on Vdd. Therefore, reducing Vdd reduces both power components. For Pdyn, the reduction is quadratic. For Pstat the reduction is linear.
- Enabling energy harvesting: Power budget reduction can allow the development of autonomous ultra-low-power devices that can be completely supplied by energy harvesting techniques. The target is to spend less power than what can be harvested from the user (e.g. watches) or from the environment (e.g. wireless sensor networks).

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Standard cell libraries using planar bulk CMOS process are optimized for super-threshold operation (i.e. Vdd > Vt). The following effects on Vt have to be considered for sub-threshold operation: (a) Drain Induced Barrier Lowering (DIBL): Vt decreases when the drain voltage of the transistor increases. In sub-threshold operation, as Vdd is reduced, the drain voltage is also reduced and DIBL is minimized. (b) Reverse Short Channel Effect (RSCE): Vt increases when the channel length of the transistor decreases. In sub-threshold operation, as DIBL is minimized, RSCE becomes dominant and long channel transistors are faster than short channel transistors. (c) Inverse Narrow Width Effect (INWE): Vt decreases when the channel width of the transistor is decreased. Therefore, to obtain higher active currents it is more effective to use transistor fingering (i.e. connect multiple transistor fingers in parallel obtaining an equivalent transistor of a higher width).

To get sub-threshold designs working, transistor models that include the above effects are required (like BSIM4 model for the 180 nm technology used in this work).

The methodology for adapting existing standard cell libraries for sub-threshold operation includes the following tasks: (a) Standard cell selection: Cells with more than 3 inputs that present the highest Ioff currents are eliminated from the library to improve the Ion/Ioff ratio (e.g. NAND4 gate). (b) Transistor sizing strategy: Channel length is upsized to 400 nm because of INWE. (c) Layout style: Layout regularity is increased (Figure 1) to reduce manufacturing process variations and to increase production yield. This task is critical for advanced technologies (e.g. 65 nm or lower). (d) Sequential cells: Clocked feedback is required for sub-threshold sequential cells like latches and flip-flops.

Figure 1: Inverter layout for the sub-threshold library.

Using this methodology, a 180 nm sub-threshold standard cell library was generated. Then, the design flow (i.e. synthesis, placement and routing) was adapted to synthesize circuits with very low frequencies and to ensure the correct operation of the circuits with both sub-threshold supply (ultra-low-power mode) and super-threshold supply (higher speed mode).

Results

The new 180 nm sub-threshold standard cell library was supplied at 0.4 V. It was used for the design of an icyflex2 processor[2] using latch synthesis. A worst case frequency of 7.0 kHz was reached with a power consumption of 7.1 μW/MHz and for an area of 0.76 mm^2. Compared with the existing low-power library supplied at 1.0 V, these results represent a sixfold reduction in energy per operation for an increase in area slightly lower than twofold which may yet be reduced. Frequency is 3 orders of magnitude lower, but only 5 times lower if the sub-threshold circuit is supplied at 1.0 V (higher speed mode) instead of 0.4 V. Moreover, working at 7.0 kHz might still be fast enough for interesting applications like blood pressure or ECG monitoring which require less than 100 Hz or 1 kHz sampling rates respectively. Finally, the supply voltage could be controlled as a function of the local threshold voltage to reduce the variations in corner cases.

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