Temperature-aware Standard Cell Design

M. Pons, J.-L. Nagel, C. Piguet

For applications where the ambient temperature varies in an important range (e.g. from -40°C to 125°C), controlling the impact of temperature variations in the circuit behavior is critical to ensure a correct operation. For the standard cell methodology in advanced technology nodes, even when temperature variation is not specifically a design constraint, circuits suffer from temperature-induced delay uncertainty that leads to failing designs. This motivates the need of investigating new temperature-aware standard cell methodologies.

Possible techniques to deal with delay uncertainty due to temperature variations are working with high threshold voltage standard cells (less sensitive to temperature) and tuning the supply voltage to the zero temperature coefficient voltage value (VTCC, where delay for a given cell is stable with temperature)\(^[1]\). Layout modifications to tune pull-up and pull-down networks to their respective temperature-insensitive operating points have also been proposed. However, each cell, for the different functions, will present different temperature-induced delay sensitivities considering the rise or fall output transitions or different input signal slews and output loads.

CSEM methodology is based on the individual evaluation of each library cell, and on the selection of a group of cells that are less sensitive to temperature variations. This group of cells is used for synthesizing the design without modifying the rest of the flow. It is expected that the circuits synthesized with this more robust cell subset are less sensitive to temperature variations\(^[2], [3]\).

Two methodologies have been selected for cell selection based on the study of the cell maximum delay sensitivity to temperature variations, depending on the cells input slew and output load combinations (that define the possible scenarios where cells will work in the design):

- MDV1 (Maximum Delay Variation method 1): cell selection limiting the maximum variation in the whole range of input slew and output load
- MDV2 (Maximum Delay Variation method 2): cells are selected only for the input slew and output load combinations where their variation is lower than the maximum allowed variation

The synthesis flow was applied to the icyflex2\(^[4]\) processor to show the delay variability reduction obtained for the worst-case delay libraries supplied in a 65 nm low power technology:

- LIB1 synthesis: Process = Slow-Slow with high-Vt transistors; Voltage = 1.08V; Temperature = -40°C and 125°C; Clock Frequency = 50 MHz
- LIB2 synthesis: Process = Slow-Slow with high-Vt transistors; Voltage = 0.9V; Temperature = -40°C and 125°C; Clock Frequency = 20 MHz

Table 1 compares the use of the complete libraries (referred as ALL1 and ALL2 for LIB1 and LIB2 respectively) vs. applying MDV1 (MDV1-LIB1 and MDV1-LIB2). The amount of cells available for the synthesis in each case and the number of different cells used are shown, as well as the total number of cells in the design and the resulting area. Finally, the average delay variability for all paths in the design is also given. It can be seen how the number of cells used is effectively reduced when reducing the set of cells available. However, it also implies an increase of the total number of cells (different combinations of cells are required to replace the cells that are eliminated) and of the final area (up to 9% for LIB1). In terms of variability, it can be seen that for LIB1, even with already very small delay variations for the reference synthesis ALL1, with the proposed MDV1 has been developed. Regarding LIB2, the average variability is not reduced (1% increase). In fact, temperature-induced variability is more critical for LIB2 than for LIB1. That is why for LIB2 the MDV2 method (that is a more fine-tuned cell selection methodology and that requires more time). Results are shown in the last row of Table 1. In this case, the reduction in variability is around 16% with a 27% area overhead.

The effectiveness of the proposals (up to 36% variability reduction with up to 27% area overhead) depends on the particular circuit and on the capacity of finding the right subsets of cells adapted to the design. Further research is required to be able to choose which method is more suitable in each case and to accelerate their automation. Moreover, the cell evaluation methodology developed gives the required guidelines to redesign the most sensitive standard cells to temperature variations.

Table 1: Results

<table>
<thead>
<tr>
<th>Subset of cells</th>
<th>#Cells used/available</th>
<th>Area (µm²)</th>
<th>Average variability</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALL1</td>
<td>188/543</td>
<td>39.9k</td>
<td>0.11ns</td>
</tr>
<tr>
<td>MDV1-LIB1</td>
<td>79/199</td>
<td>43.4k (+9%)</td>
<td>0.07ns (-36%)</td>
</tr>
<tr>
<td>ALL2</td>
<td>216/543</td>
<td>42.4k</td>
<td>2.15ns</td>
</tr>
<tr>
<td>MDV1-LIB2</td>
<td>108/252</td>
<td>43.5k (+3%)</td>
<td>2.17ns (+1%)</td>
</tr>
<tr>
<td>MDV2-LIB2</td>
<td>227/492</td>
<td>53.9k</td>
<td>1.79ns (-16%)</td>
</tr>
</tbody>
</table>

Research was partially funded by EU FP7 ICT Therminator project.